

A new infrared camera for COAST

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ABSTRACT

We describe the design of a new IR camera for the Cambridge Optical Aperture Synthesis Telescope that has been designed both to increase our science productivity at COAST and to prototype novel hardware architectures for the Magdalena Ridge Observatory Interferometer IR detector systems. The new camera uses a Rockwell HAWAII sensor in place of the NICMOS device from our previous camera and will be able to sample the temporal fringe patterns from the four outputs of the COAST infrared beam-combiner at frame rates up to 10 kHz. The use of non-destructive multiple reads should allow an effective read noise of 3 electrons to be attained with this chip. The camera controller uses a PulseBlaster FPGA card to generate the timing signals: the advantages of this are flexibility, ease of use, and rapid reconfiguration of the clocking scheme. The new system should improve the IR sensitivity of COAST by around 2 magnitudes. We detail the design of the hardware and the associated software.

Keywords: COAST, MRO, infrared camera, Rockwell Hawaii, PulseBlaster, QuickUSB

1. INTRODUCTION

We describe the design, and rationale for a new infrared camera at COAST, the Cambridge Optical Aperture Synthesis Telescope^[1]. This camera replaces the existing NICMOS-based system with a Rockwell HAWAII 2.5-based camera, and will increase science productivity at COAST as well as being a prototype for an IR detector system at the forthcoming Magdalena Ridge Observatory Interferometer^[2] in New Mexico. The new camera will be able to simultaneously sample the temporal fringe patterns from the 4 outputs of the COAST infrared beam combiner at frame rates up to 10 kHz. By using non-destructive multiple reads, we aim to obtain an effective read-noise of 3 electrons. This should improve the IR sensitivity of COAST by approximately 2 magnitudes. The camera system is designed for ease of use, flexibility, and to permit rapid reconfiguration of the readout clocking scheme. In this paper, we first describe the COAST and MRO telescopes; then we compare the differences between the NICMOS and HAWAII sensors; lastly we describe the new hardware design, and the rationale behind it.

1.1. COAST - the Cambridge Optical Aperture Synthesis Telescope

The Cambridge Optical Aperture Synthesis Telescope is a long-baseline 5-element interferometer which has the ability to measure closure phases. It can obtain images by earth-rotation aperture synthesis. The telescope may be configured to use baselines up to 100 m, providing a resolution of 1 milli-arcsecond. COAST operates in the red and near infrared wavelengths between 600 nm - 2.3 μm ; it has a limiting magnitude of 6.4 in the I-band. Each siderostat comprise a 40 cm Cassegrain telescope, with a moveable flat mirror for pointing; up to 4 of the 5 may be used simultaneously. COAST is located at the Lord's Bridge site in Cambridge, and was the world's first optical/IR interferometer to obtain images by aperture synthesis. COAST is now also used as a test-bed for new technologies at the forthcoming Magdalena Ridge Observatory.

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Figure 1 shows the operation of COAST. The 4 selected siderostats are automatically guided to track the star and collect its light. The light beam is then reduced in diameter, and sent through a beam-pipe into the optics laboratory. The optics laboratory is inside a bunker covered with earth and grass - this makes it extremely thermally stable. Within the optical laboratory, the light is processed as shown in Figure 1. The incoming beams first undergo path-compensation: the optical path lengths are equalised by moveable mirrors, mounted on trolleys. The trolley position is itself tracked to high precision by a laser interferometer. The phases are then equal, with the exception of the phase error introduced by the atmosphere. When 3 or 4 siderostats are in use, it is possible to obtain the closure phases.

The four beams are then combined, resulting in interference fringes. Red light is detected by 4 avalanche photo diodes; infrared is detected by 4 pixels of the IR camera, which is used as a detector, as opposed to an imager. The outer annulus of the light is used by the auto-guider to track the star.

The trolleys sweep back and forth every 100/250 ms to encode temporal fringes. The typical fringe frequencies are 250 Hz (IR) and 700 Hz (optical). The data is then stored and reduced by a computer, and using earth-rotation aperture synthesis, it is possible to reconstruct an image of the object under observation. Many significant astronomical results have been obtained^[3].

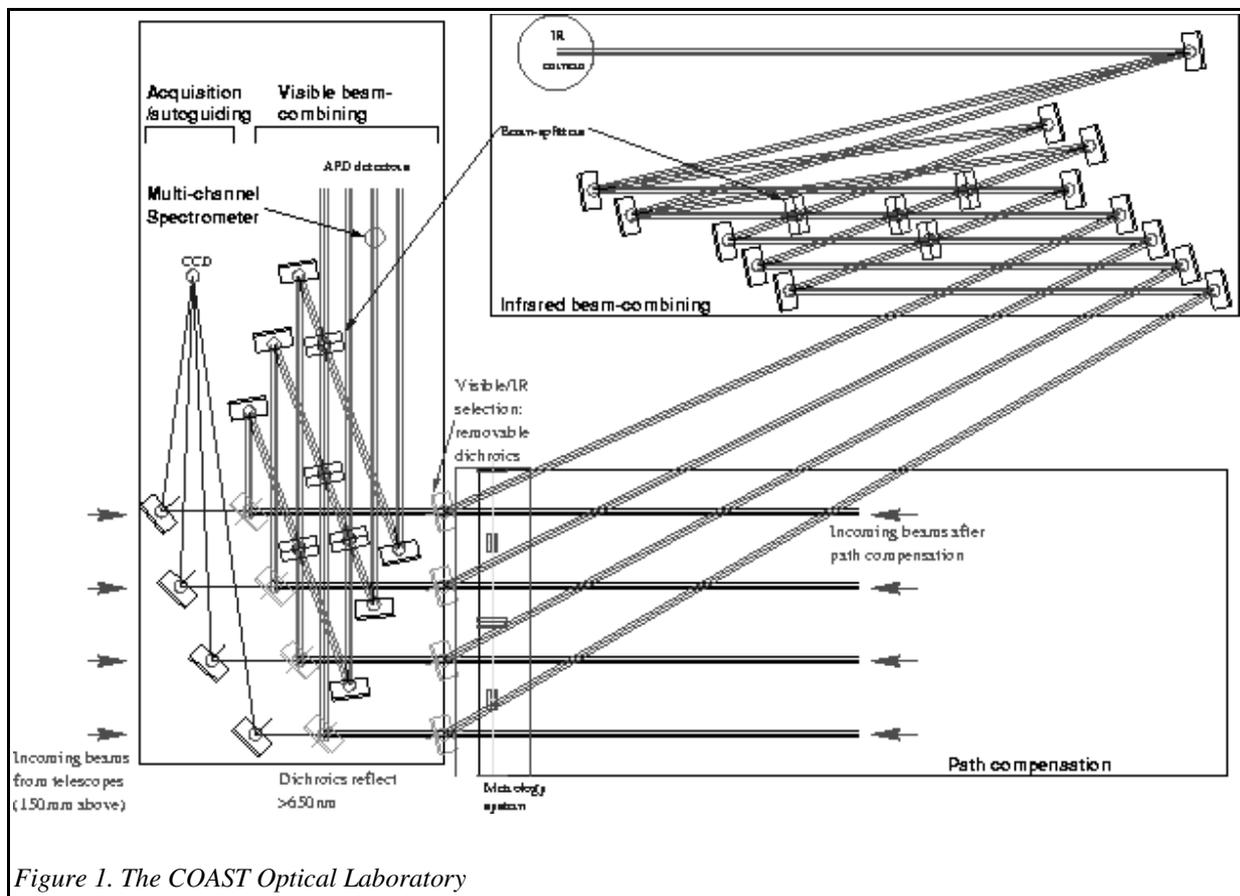


Figure 1. The COAST Optical Laboratory

1.2. MRO - the Magdalena Ridge Observatory

The Magdalena Ridge Observatory Interferometer (MROI) is a facility class interferometer, whose design is based upon our experience at COAST. It is located in New Mexico, at an altitude of 3.2 km above sea level, and will be completed in 2008. MRO will have a single large 2.4 m telescope, and an 8-10 element optical/infrared interferometer. The interferometer will have 1.4 m diameter mirrors, arranged on variable baselines up to 400 m. The resulting array will operate between 0.6-2.4 μm : it will have very high sensitivity and an extremely high angular resolution of $\frac{1}{4}$ milli arcsecond. The Magdalena Ridge Observatory will be used to study the formation of planets, stellar accretion and mass loss, and active galactic nuclei.

The Magdalena Ridge Observatory project is an international scientific collaboration between New Mexico Tech, the University of Cambridge (UK), New Mexico State University, New Mexico Highlands University, the University of Puerto Rico, and Los Alamos National Laboratory. The project is overseen by the U.S. Naval Research Laboratory.

1.3. The NICMOS camera

The existing camera, designed and built by Martin Beckett^[4] using a Rockwell NICMOS sensor and an AstroMed controller was "state of the art" when it was built 9 years ago. Using correlated double sampling (CDS), it is capable of reading 4 pixels once each at 1 kHz, 2 pixels once each at 2,5 kHz, or 16 multiple reads of a single pixel at 1 kHz. This is insufficiently fast to obtain closure phases when using all the available light (i.e. all 4 of the combined beams) at COAST. The read noise is 16 electrons for single reads; this can be reduced to approximately 8 electrons when reading only a single pixel, using 16 multiple reads with no reset between frames (and the consequent reduction of dynamic range). Observations have been made at an H-magnitude of 2.5. A notable achievement of this system was the first infrared image made from an aperture synthesis array, of the binary star Capella in 1997^[3].

However, there are some disadvantages of the NICMOS system. It suffers from a low readout rate, and relatively high noise, compared to current technologies; spares are unobtainable, and the AstroMed controller is obsolete. The system is also somewhat less than user friendly: modifications to the clocking scheme require that changes are made to the assembly code for the controller, and the entire system is MS-DOS based, making remote control of the system over a network impractical.²

1.4. The Hawaii camera

The new Hawaii-based system uses a Rockwell Hawaii-2.5 focal-plane array sensor which has a read-noise below 3 electrons (for multiple reads with CDS), and will be able to be read out much faster. At COAST, we aim for a frame rate of 10 kHz with many multiple reads; faster at MRO. An imaging mode will be required for alignment and calibration of the system; spectroscopic readouts will be possible by using multiple pixels and a diffraction grating. The 4 quadrants are each be clocked quasi-independently, allowing pixels with different co-ordinates to be used in each quadrant. This permits the selection of the best pixels, and avoids an optical alignment criticality. Each quadrant has its own analogue electronics (amplifier, integrator, sample-and-hold, analogue-to-digital converter), so that a 4-fold improvement in data-rate or multiple reading is possible. The new system will be Linux-based and will have improved software, user-interface and networking capabilities. The design is described below.

² Once the camera application is running, the application may be controlled over a serial link. However, control of the operating system itself is not possible in this manner.

2. HARDWARE DESIGN

2.1. Design overview

The block diagram of the system is shown in Figure 2. The arrows represent the direction of information flow.

The Hawaii focal-plane-array detector is located in a dewar and cooled to 78 K using liquid nitrogen. No other electronic components, save some decoupling capacitors are present in the dewar: we decided against cryogenic amplification as being unnecessary. The light from the beam combiner passes into the dewar and through one of several filters selected from a filter-wheel to allow additional control of the spectral band-pass. The light is focussed onto the detector: each of the 4 beams contains the same information and one quarter of the total light, and is concentrated onto a single pixel, one beam per quadrant.

The camera is controlled from a master computer, which is placed at some distance from the optics, and which interfaces to the COAST data manager. This is also the server from which the thin-client mini-itx diskless, fanless computer is booted. The mini-itx computer contains a PulseBlaster PCI digital timing card, which emits the clocking signals for the detector and ADC, according to a pre-determined pattern, and synchronised with the COAST master-clock. These clocking signals are transferred to the Hawaii sensor via electrostatic discharge protection and level-shifting; they pass into the dewar on wires of low-thermal conductivity.

Every sweep of the trolleys (usually 250 ms) restarts the clocking sequence. The PulseBlaster resets the array addresses, and then initiates a correlated double sampling scheme³ (Reset, Read, Wait, Read) with multiple reads each time. Each sample is integrated to reduce noise; it is then passed to a sample-and-hold circuit and then digitised. The clocking scheme, integration time and gain may be varied.

The output from the camera is amplified, integrated, digitised, and then loaded into a large-capacity FIFO buffer, which can store up to an entire frame of data in imaging-mode. The data is then read into the mini-itx computer via the QuickUSB module (acting as a fast parallel port). The data is then sent out through the control computer and over the network. The aim is for an overall latency of less than 10 ms, so that feedback control of the telescope is possible.

The mini-itx system was chosen to minimise heat emissions and vibration in the vicinity of the optics. The PulseBlaster has its own FPGA to which is programmed with the clocking schema: it is independent of its host while running. This minimises jitter, and eliminates the need for an operating system with hard-real-time capabilities. It also allows for quick changes to the readout mode if desired.

2.2. Rockwell Hawaii FPA sensor

The camera is based upon a Rockwell Hawaii⁴ 2.5 μm CMOS HgCdTe Focal Plane Array^[5]. This array consists of 1024 x 1024 pixels, each 18.5 μm across, arranged in 4 identical independent quadrants. It is designed to minimise glow and dark current, and it operates at a running temperature of 78 K (liquid nitrogen) and a cut-off wavelength of 2.5 μm . The hybrid sensor consists of a mercury-cadmium-telluride infrared detector, bonded onto a heavily-doped CMOS silicon multiplexer. We have an engineering-grade sensor, kindly loaned to us by the United Kingdom Infra-Red Telescope (UKIRT). It is necessary to design and construct our own controller for this sensor.

³ Correlated double sampling (CDS) is explained further in section 2.8

⁴ Note that the Hawaii 2.5 detector is an earlier product, and is not the same as either of Rockwell's current detectors, the similarly named Hawaii-1RG and Hawaii-2RG.

Each pixel of the detector has a full-well capacity of 10^5 electrons and a gain of 3.4-6.8 $\mu\text{V}/\text{e}$. Using 16 bits of analogue-digital conversion covers almost the entire range without the need for adjustment of the gain. The read noise is < 3 electrons for Fowler sampling (multiple reads).

Each quadrant of the CCD receives one beam from the beam-combiner, and the pixels upon which these beams fall need not have the same coordinates: the quadrants operate quasi-independently, and each has its own analogue circuit. The FrameSync clocks are commoned out of necessity (the PulseBlaster has only 24 outputs, whereas 27 would be needed), however this would be desirable anyway: resetting, or clocking one quadrant while reading from another would tend to introduce interference.

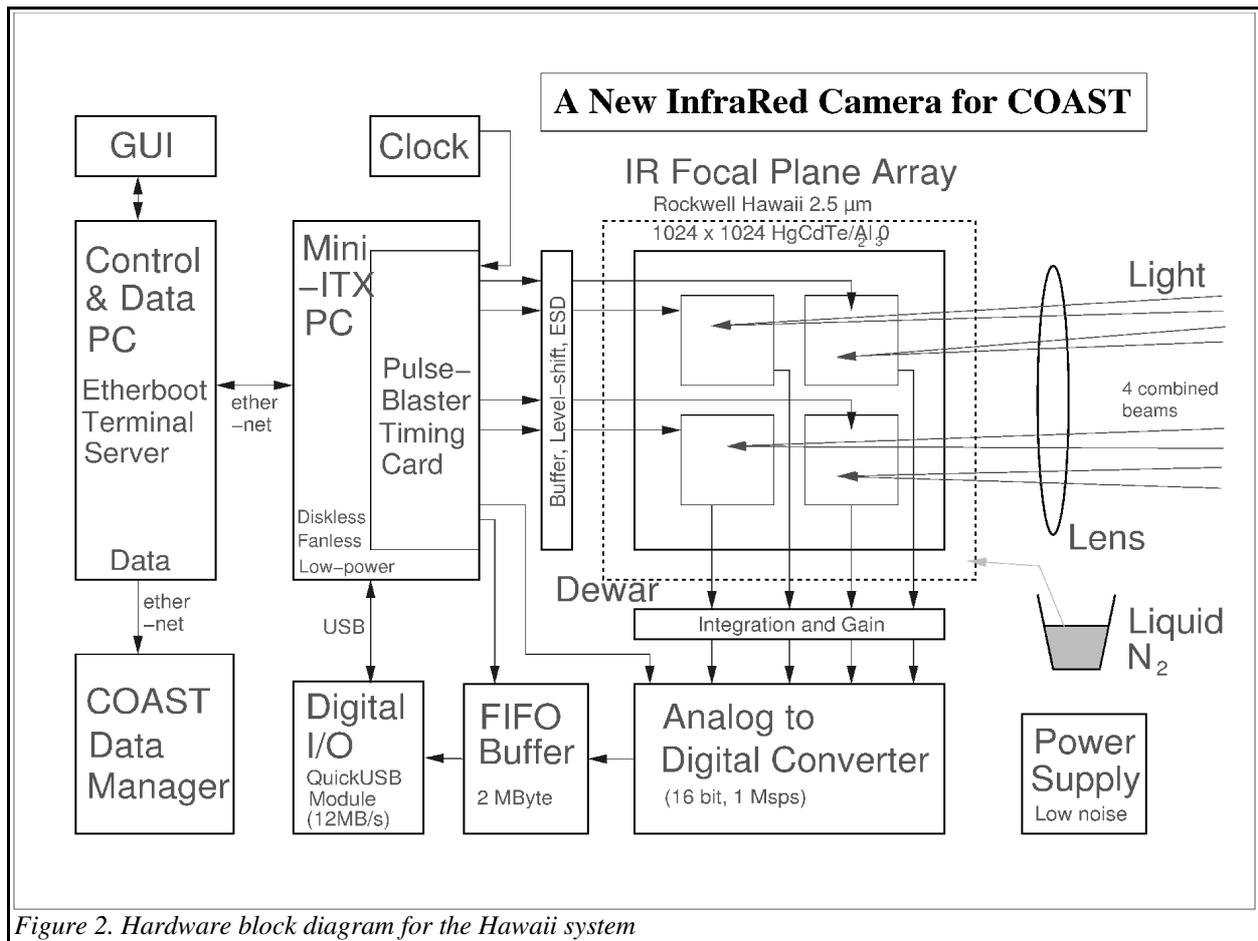


Figure 2. Hardware block diagram for the Hawaii system

2.3. Analogue circuit and ADC

The output from the Hawaii chip is at a low-level, and so we need to amplify and filter it. The gain is calculated from the specified sensitivity of the Hawaii chip (between 3.4-6.8 $\mu\text{V}/\text{electron}$), its well capacity of 10^5 electrons, and the use of a 16-bit analogue-to-digital converter. The resulting requirement is a selectable gain in the range of 7-40. This provides, at the high end, 1-bit resolution at a level better than 1 electron; at the low end it prevents going off the end of the 16-bit scale before the detector is saturated.

We have selected the Analog Devices AD8021 op-amp^[6] to provide the necessary gain: this has a specified noise of 2 μ V at 1 MHz, less if bandwidth limited, which is well below the minimum output from the detector for a single electron. This is comparable to the Johnson noise of a 60 Ohm resistor at room temperature. Cryogenic amplification was considered, but is not necessary in this application, and would add considerably to the cost and complexity.

The output from the Hawaii sensor also contains a lot of high frequency noise^[7]. Therefore, it is desirable to average this signal over the entire readout time by using an integrator. This means that a sample-and-hold circuit is required between the integrator and the ADC. The sample-and-hold circuit, and the ADC triggering are controlled from the PulseBlaster.

Depending on the readout mode, it is necessary to be able to vary the time-constant of the integrator - which also has the side-effect of varying its gain. This means controlling both the feedback capacitance, and the input resistance, which is effected by means of FET analogue switches to switch extra capacitors and resistors in and out of the circuit. FET switches such as the Analog Devices ADG712^[8] are effectively ideal, with typically a 2.5 ohm on-resistance, 0.01 nA leakage current, and a switching time of 10 ns.

The analogue-to-digital converter we have selected is the Analog Devices AD7677^[9] chip, designed to be paired with the Analog Devices 8021 op-amp. This is capable of 16-bit conversion at 1 Msample/sec, and a reasonable power consumption of 115 mW. All 4 ADCs are triggered simultaneously, so that the noise generated by one conversion and read-out does not affect the signal to another.

2.4. Digital Circuit

Once the analogue-to-digital conversion has taken place, the 4 ADCs are read out, in sequence into a FIFO buffer. Although it is not necessary to have such a large buffer for the current application, we foresee the potential use for storing an entire image-worth of data. Therefore, the FIFO is 2 MByte in size (1024 x 1024 x 16 bit), comprising 2 of IDT's 72T18125^[10] FIFOs in a daisy chain. The data is then read into the control computer via the QuickUSB module, discussed below, which handshakes with the FIFO to detect over and under-flows.

2.5. Thin-client camera control computer

The camera electronics receives its timing signals from the PulseBlaster, and needs to send the data back over USB. Neither of these are capable of long-range transmission (except by using Low Voltage Differential Signalling (LVDS), which would significantly add complexity), therefore it is desirable to locate the control computer near to the camera. The data is then sent via ethernet to the data-manager computer for storage and further processing. However, this means that the vibration and heat dissipation in the vicinity of the optics must be low. Therefore, we have selected a diskless, fanless thin-client computer as to act as the controller. We decided upon the VIA Epia ME6000^[11], because it is low cost, requires only 4 Watts, and has the required capabilities of 10/100 Ethernet and USB 2.0 interfaces. It is booted via the network using the Etherboot software, which we now describe.

Etherboot^[12] allows any computer with a modern BIOS to load a kernel over the network, and use this to boot. The client first obtains an IP address by DHCP; the DHCP server also tells it the IP address of the machine from which to load a kernel, the Network File System (NFS) path, and the kernel command-line. The client then loads a network boot-ROM image^[13] via trivial file transfer protocol (TFTP), and this in turn loads a kernel from NFS. The machine then continues to boot Linux in the normal way, except that its file system resides upon the server. The system may then be used as a thin client (running only an X server), as a medium client (running applications locally), or as in our case, headless, with remote login via SSH, and /home mounted as a ramdisk. By default, NFS makes the server's entire root partition available as 'ro,all_squash' (read only, with the access rights of 'nobody'), so the client effectively runs with exactly the same configuration as the server. This can be modified by the configuration files to define the client's setup

and services; for example by changing the directory: `/etc/rc3.d$$CLIENT$$/`.

Etherboot is GPL (Free) software; we are using the Fen Systems^[14] package 'nymph' running under Mandrake Linux 9.2^[15] and a 2.4.22 kernel. This works very well, but for one strange bug: after the network bootable image has loaded, while the Linux kernel is booting, and obtaining an IP address for itself (running DHCP for the second time), there were Ethernet PHY timeouts, and 'complaints' about missing network media. This was tracked down to ACPI; and since the Epia ME6000 has no BIOS option to disable ACPI, it was disabled from the server in `/etc/dhcpd.conf` with `'option etherboot.kernel-cmdline " devfs=mount acpi=off";'`

2.6. PulseBlaster digital timing card

To generate the clocking signals for the camera, we are using Spincore's PulseBlaster^[16] FPGA-based PCI digital timing card. This emits a programmable stream of pulses on 24 output channels with 10 ns resolution, and a minimum pulse length of 90 ns. It can be started and reset in software, or from external hardware triggers. At COAST, the PulseBlaster is triggered from the master clock, so as to be synchronised with the trolley sweeps; it then controls the clocking of the camera to obtain the desired readout mode. The PulseBlaster is programmed with 32 k of 80 bit VLIW (Very Long Instruction Word) RISC instructions, each of which contains an op-code, the output data, the subsequent delay, and an optional address. The instruction set is extremely limited (delay, longdelay, loop, endloop, goto, call, return, wait, stop), but adequate. In particular, it contains no conditional jumps, which are unnecessary in a triggered sequencer, and no bitwise operations, a limitation addressed by our parser. Once the program has been uploaded over the PCI bus, the PulseBlaster is independent of its host, requiring no CPU resources, and no realtime capability from the OS. In fact, it will even continue to operate during a reboot!

For each quadrant of the sensor, we separately control Lsync (line reset), Line (vertical clock), Pixel (horizontal clock), ResetB (line reset) and Read. The FSync (Frame Sync) lines are ganged together so as to free up 3 output lines of the PulseBlaster to control the ADC start-conversion-trigger and the integrator's sample-and-hold control/reset. The PulseBlaster has 3.3 V TTL outputs which are connected directly to the camera via level-shifting and electrostatic discharge protection circuitry.

The PulseBlaster has an excellent GPL'd^[17] Linux driver, but expects to be programmed in hexadecimal; therefore we have written an assembler/parser for it so as to make it easier for humans to write the program files. For example, our parser supports: labels (instead of numeric addresses); human-readable values (data in hexadecimal, decimal or binary, times in ns, μ s, ms as well as cycles), includes, defines, debugging, functions, and bitwise operators (set-bits, clear-bits, AND, OR, XOR). It also deals with some peculiarities, such as the offset values for delays required by the PulseBlaster. The advantage of the PulseBlaster being a sequencer, rather than Turing-complete, is that it is easy to step deterministically through the sequence. This means that the extra opcodes can be "fudged" by the parser, based on a knowledge of the previous state. For example, in pseudocode: "output 0xFFFFF00; bitset bit_0;" is converted by the parser to "output 0xFFFFF00; output 0xFFFFF01;".

The parser is written in the PHP scripting language, and is Free Software, released under the GNU General Public License.

2.7. QuickUSB digital I/O

The Hawaii sensor is capable of a very rapid readout rate; the system is designed to work at up to 1 MHz, although in practice, this will probably not be used. On 4 quadrants, at 16 bits each, this provides a data rate of up to 8 MByte/sec. It is a 1 megapixel (1024 x 1024) sensor, so there is a 2 MB FIFO buffer capable of storing an entire frame. However a fast, sustained data rate is required. Most interfaces such as serial (RS-232), parallel (RS-245), GPIB, USB-1.1 are not capable of providing this, and faster interfaces such as ethernet and firewire are hard to build custom interfaces for. We

have selected the QuickUSB^[18] module from Bitwise Systems as the solution. This device is a USB-2.0 module, capable of acting as essentially a fast parallel port, at up to 16 Mbyte/sec sustained. It also has some extra ports for general purpose use, and is capable of handshaking with a FIFO. The QuickUSB module is supplied with Linux drivers (via LGPL'd libusb^[19] library), and with its own set of high-level C++ libraries (libquickusb.so). The supplied libquickusb libraries are proprietary, closed source, and somewhat buggy, so we are working on reverse engineering them and will release a GPL'd library.

2.8. Noise considerations

The reduction of random noise is of great importance, when aiming for high sensitivity. This entails careful selection of components, especially in the pre-amplifier. Thermal Johnson noise is also problematic, although not sufficiently so as to require a cryogenic amplifier, with all its complexities. The Hawaii sensor also acts as a source of noise. One source of noise is the internal “glow” of the device: internal power dissipation causes infrared emission within the same band to which the detector is itself sensitive! This can be largely mitigated by disabling the output source-follower for a large proportion of the operating duty-cycle. External interference is also a problem: this is mainly introduced by radio-frequency interference, and mains-hum. Shielding, careful power-supply design (using linear regulators, and toroidal transformers, not switch-mode regulators), ground-planes, and minimising loop areas for electromagnetic coupling are all necessary.

The prevention of systematic and repeatable noise is not necessary, because it may be compensated for: for example, the reset noise of the detector. This arises because resetting a pixel does not set it to a precise and exactly repeatable level. However, the use of correlated-double-sampling (CDS) can overcome this. CDS works as follows: [1.] The pixel is reset to some level (near, but not exactly zero, unknown). [2.] The pixel level is immediately measured (value=X). [3.] The detector is allowed to collect light for a period of time. [4.] The pixel level is measured again (value=Y). [5.] The amount of light received may be calculated from the difference (Y-X), thereby removing the effect of the unknown reset-level. Even this CDS is not perfect, because there is some noise inherent in each read. However, since the reads are non-destructive, each read may be performed multiple times, thereby reducing their error. Another source of error is the induced interference between parts of the circuit. For example, when the A-D conversion takes place, a spike is usually created on the power supply. This can couple into the signal. However, because the ADC spike is precisely repeatable between one conversion and the next, it may be subtracted out. This reduces the criticality of the design in separating the digital and analogue parts.

3. CONCLUSIONS

We have described the design of the New Infrared Camera for COAST, and the reasons why these particular design choices have been made. We have also described the software which we have written, copies of which may be obtained from the author. It is worth noting that the availability of high performance electronic components and software at low cost and free respectively is of key importance to this design.

The final system, test results, and resulting astronomical measurements will be the subject of another paper, and will also form the author's PhD thesis. It is intended that everything will be fully documented on the Web, and thus made available to other scientists.

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