Silicon Nanostructures

A Thesis Submitted to the
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for the Degree of
Master of Philosophy

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To Claire with love.

Abstract

Silicon nanowires have great potential in both physics and microelectronics. This research investigates the low temperature methods available for growing nanowires via the radio-frequency plasma-enhanced chemical vapour deposition of silane. The use of gallium was not possible; however the gold-silane vapour-liquid-solid method proved successful for growing thin nanowires. The growth conditions were optimised: the most successful were a 0.5 nm thick layer of gold heated to 400 ^{o}C (nominal) at a pressure of 1500 mTorr for 90 minutes. A gas flow of 80 sccm of pure silane was used and decomposition was assisted by 6 W of RF plasma. This yielded dense, crystalline silicon nanowires up to 30 μm in length and as small as 10 nm in diameter.

Declaration

I hereby declare that my thesis is not substantially the same as any that I have submitted for a degree or diploma or other qualification at any other University. I further state that no part of my thesis has already been or is being concurrently submitted for any such degree, diploma or other qualification.

Signed: _____ Date: _____

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1 Introduction

Silicon nanowires have exciting potential for both theoretical physics and in microelectronics. From a physics perspective, the wires are of interest because they exhibit quantum confinement, and are quantum-mechanically one-dimensional solids. Thus they take their place among low-dimensional research between zero-dimensional quantum dots, and two-dimensional electron gases.

From the perspective of microelectronics, the nanowires have the ability to emit light effectively, in contrast to bulk silicon. This allows optical components to be easily incorporated onto silicon wafers, with the potential for extremely fast computing. The silicon may also be doped. Other potential applications include sharp tips for field emission (electron microscopy, field-emission displays); interconnects, logic gates and memory for nano-electronics; and advanced battery technology: doped with lithium, the nanowires have an extremely high surface area for chemical reactions. Although no commercial applications yet exist, these possibilities have all been experimentally demonstrated, and research proceeds at a rapid pace.

The aim of the experimental work recorded herein is to grow, if possible, pure, densely packed, long, straight, vertically-aligned, thin silicon nanowires. This thesis concentrates upon one of the possible methods for growing silicon nanowires, the vapour-liquid-solid (VLS) method, and the ways in which it may be optimised. Different process methods: gas mixtures, pressures, and the presence or absence of plasma are considered, as are the effects of using different metal catalysts, and the thickness of the catalyst metal layer. In particular, the gold-silicon VLS method is investigated.

In the first section, the applications of silicon nanowires are reviewed in greater detail, and the methods for their growth as reported in the literature are surveyed. In the second section, the relevant theory is introduced: the Au-Si reaction, conditions for growth of amorphous versus microcrystalline silicon, RF-plasma-enhanced chemical vapour deposition and the effect of temperature and pressure on the nanowires. The third part covers the actual experimental methods used for growth and analysis of

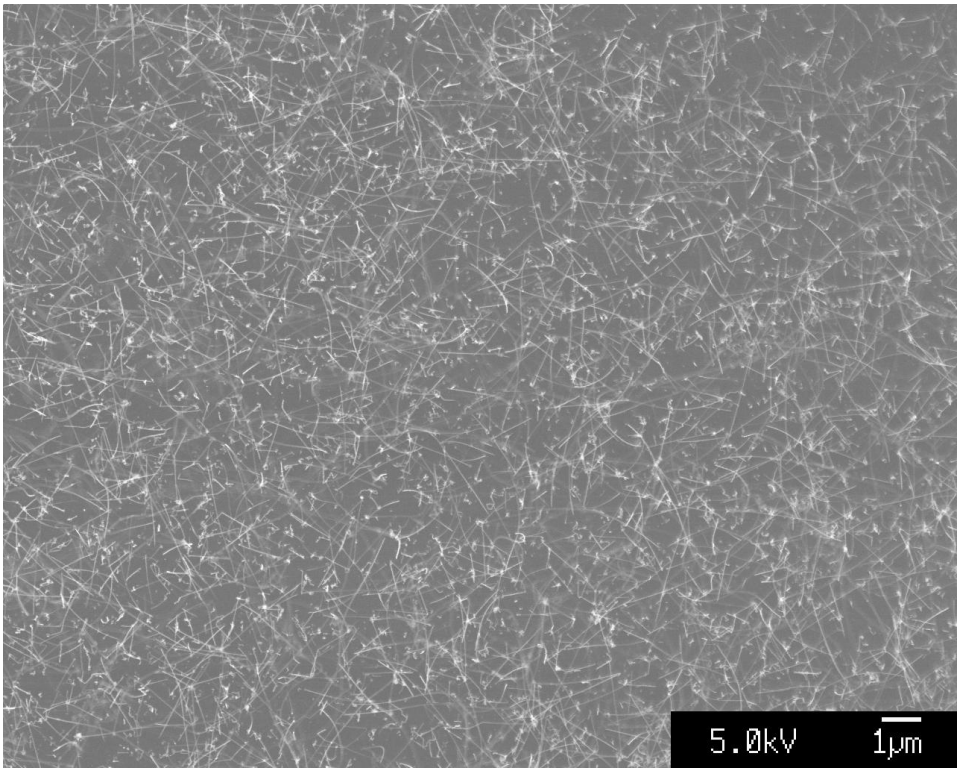


Figure 1: Silicon nanowires grown using plasma enhanced chemical vapour deposition of silane with a $\frac{1}{2}$ nm thick gold catalyst layer.

the resulting nanowires. In the fourth section the wires are analysed by microscopy. Finally, the implications are discussed and conclusions are drawn.

1.1 Silicon Nanowires and their Applications

Silicon nanowires are typically between 3-20 nm in diameter and 1-30 μm long. This corresponds to approximately 150 atoms across and 2×10^5 atoms long: an aspect ratio of ~ 1000. They are internally pure silicon, although sometimes coated with oxide (which may be removed with $HF_{(aq)}$). The wires are usually single crystals, forming straight wires, although sometimes they have defects causing kinks[1]. Figure 1 shows some 10 nm wide and 5 μm long nanowires grown during the research performed for this thesis. Unlike carbon nanotubes, the silicon nanowires are solid rods. They are also always semiconducting, and can be doped with B, P, Al or other atoms. This gives them far more predictable properties than carbon nanotubes, which are randomly semiconducting or metallic, depending on the manner in which the graphite sheet is rolled up[2]. Some key possibilities of silicon nanowires are now introduced.

1.1.1 1-Dimensional Systems

Low-dimensional systems have interesting properties, both theoretically and practically. In the case of silicon nanowires, the wire is not quasi-one-dimensional, but is purely one-dimensional in a quantum-mechanical sense[2]. What this means is that the wavefunction varies only along the length of the wire,

and not across its width. There is a critical radius for nanowires, below which they may be considered purely one-dimensional: an illustration of this is given in appendix A. Such one-dimensional systems have unusual properties, such as density of states singularities, spin-charge separation, and discrete molecular-like energy levels extending over large lengths. This permits theories to be tested in unusual regimes, and materials with properties such as very high tensile-strength to be created.

1.1.2 Silicon Lasers

Bulk silicon is an indirect bandgap material. Thus, for the emission of a photon, a phonon must first be absorbed: this makes it an extremely inefficient emitter of light. However, due to quantum confinement, the k-selection rules are changed for nanometer-scale silicon, and it can emit light. Silicon nanowires, nanocrystals, and highly porous silicon can all emit light, with an efficiency which currently stands at 1%[3].[1] The smaller the size of the silicon, the better it can emit light: for efficient emission of blue light, calculations require crystals of size 1 nm. Nevertheless, Si-LEDs are slow (switching times $\sim 1\ \mu$s), since the nanocrystalline silicon retains some of its indirect-bandgap character. Quantum confinement is also responsible for a dramatic increase in the optical gain of the silicon, allowing it to compete with direct-bandgap materials[4]. Combined with stimulated emission, which further enhances the response time, nanocrystalline silicon lasers can switch at the GHz frequencies required for fast computing and optical communications. Such lasers can be easily integrated onto silicon integrated circuit wafers, allowing far greater ease of fabrication than is currently possible using GaAs optics.

Figure 2 shows how the theoretical size of the energy gap is increased for small silicon nanoclusters[5]. The bandgap increases by a factor of ~ 8 between bulk silicon and a 1 nm nanocluster. The lines shown are calculated by two different approximate methods: the local density approximation, and the quantum Monte Carlo method. A further explanation of why quantum-confined silicon makes a good light emitter is given in appendix B.

1.1.3 Sharp Tips

In common with carbon nanotubes, silicon nanowires have applications as atomically sharp tips in scanning electron microscopes, surface profiling, and field emission. They may also be used as the interconnecting wires in nanoelectronic devices. However, silicon has some advantages over carbon. Silicon nanowires are always semiconducting, and may be doped. This means that they have reliable, repeatable electronic properties. Their size and location may be precisely controlled[6, 1]. Furthermore, field emission tips may easily be created on the same silicon wafer as the active and control elements. For instance, a field-emission display may have the HV-CMOS drive electronics and the field-emission tips integrated cheaply onto a single wafer.

[1] This 1% is the ratio of emitted photons to injected electrons.

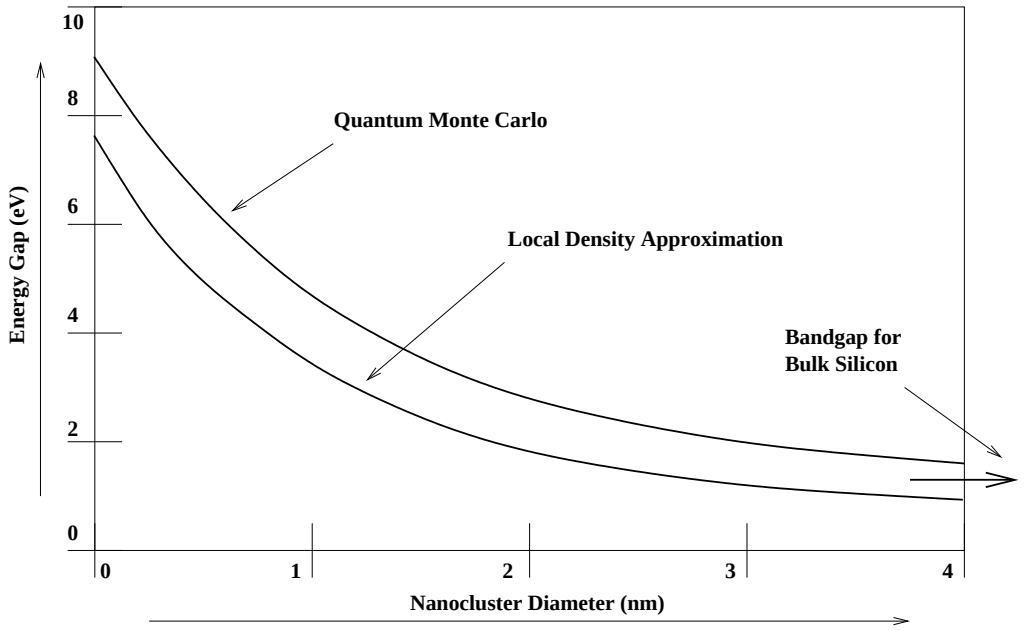


Figure 2: As the nanowire becomes smaller, the energy gap increases from its bulk value.

1.1.4 Crossed Nanowire Electronics

Unlike carbon nanotubes, which are randomly semiconducting or metallic, the electronic properties and sizes of silicon nanowires can be precisely controlled during synthesis[7]. These can be doped (p-Si and n-GaN), and precisely manipulated by microfluidic alignment.[2] Thus nano-scale p-n junctions, field-effect transistors and logic gates are possible - a half-adder has been demonstrated[7]. Hetero-junctions of metallic carbon nanotubes and (semiconducting) silicon nanowires can form Schottky diodes[9]. A grid of crossed nanowires may be electrically addressed by row and column, and contains p-n junctions at each intersection. Such junctions can have areas of 1 nm^2, and may be spaced at 5 nm: this permits an extremely dense array of LEDs, photodiodes, or memory elements. Possible applications include photo-lithography, sensors (cameras, particle detectors, microscopy), and programmable read-only-memory[8].

1.1.5 Other

Nanowires have an extremely high surface area. Doped with lithium, silicon nanowires may be used for electrodes in high-performance batteries. The high surface area for Li+ ion absorption make possible a very high energy density and a fast charge/discharge rate[10]. Precisely doped silicon nanowires have been used for ultra-sensitive chemical and biological sensors: individual ions and proteins may be sensed in real time. High resolution imaging of nucleic acid may lead to real-time sequencing of DNA, and "diagnosis on a chip"[11].

[2] The nanowires are removed from their substrate by ultrasound. They are dissolved in ethanol and then drawn through fine channels in a hydrophobic polymer by capillary action. This causes them to align. Channels may be crossed over, giving junctions, and gold may be deposited to make electrical contact. [8]

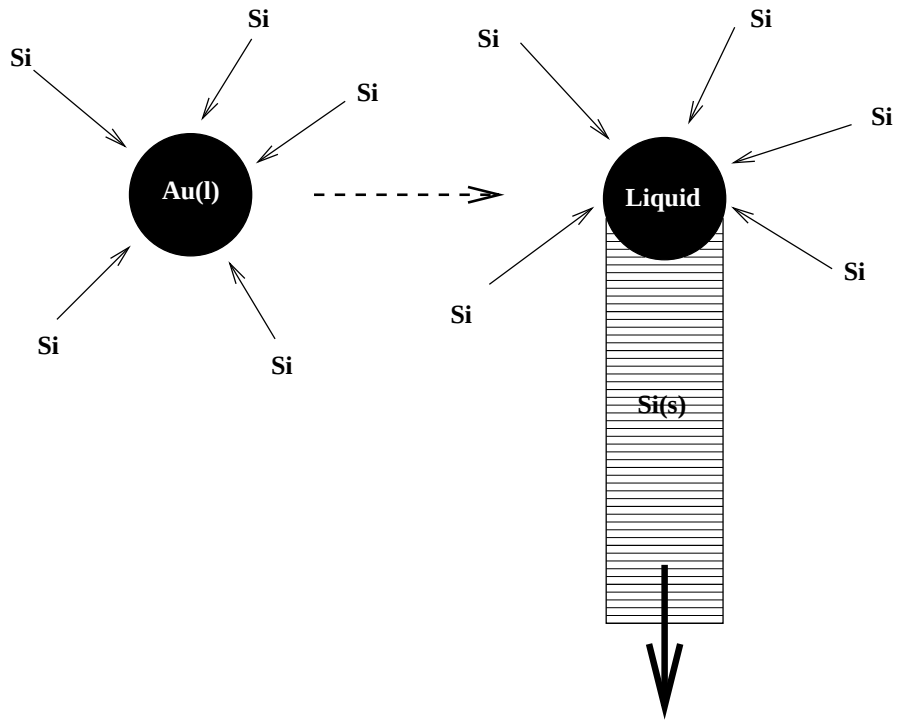


Figure 3: The ball of molten catalyst acts as the growing point, and defines the nanowire diameter. The ball size is typically 1-2 nm larger than the wire.

1.2 Growth of Silicon Nanowires

Almost all the methods for growing silicon nanowires incorporate some aspect of the "Vapour-Liquid-Solid" (VLS) method. In this method, a liquid alloy cluster mediates between the gas and solid phases: it serves to absorb atoms from the vapour, and then precipitates them out as a solid wire.

The nanowire raw-material, Si, is supplied as a vapour, typically as SiH_4, although the source can be $SiCl_4$[1] or a laser-ablated metal-silicon compound such as Fe-Si. The growing point is a molten ball of alloy: a mixture of catalyst and silicon. The catalyst, usually Au or Fe, preferentially absorbs the reactant and aids its decomposition. The catalyst then supersaturates with silicon, and is the nucleation site for crystallisation. Finally, the silicon precipitates out of the catalyst, growing into the solid wire[2]. This is shown in figure 3. There is a longer explanation of the eutectic and silicide reaction mechanisms in section 2.1. The catalyst ball must remain liquid for growth to continue, however the silicon wire must be solid. For these phases to co-exist, the catalyst and the silicon must form a molten eutectic or alloy. Because the size of the ball of catalyst determines the nanowire diameter,[12] the catalyst must exist as nanometer-scale clusters of atoms. Thus, to grow nanowires, the following are required:

- The temperature, pressure and catalyst must be such that the catalyst forms a molten eutectic or liquid alloy which co-exists with solid Si, and the source gas decomposes. These can be predicted from the metal-catalyst/silicon equilibrium phase diagrams.

- The catalyst must exist in nanometer-sized balls, either by spontaneously forming droplets, or by pre-existing at that size. It is this condition that is the most difficult to arrange, and which requires experimental ingenuity.

The type, density, crystallinity, length and quality of the wires that result depend on many factors, including: temperature, pressure, gas mixture, catalyst thickness and patterning, electric field, and presence or absence of plasma: the effect of these variables is discussed later. There now follows a summary of the various methods that have been reported for growing nanowires, grouped together by the way in which the catalyst nanoclusters are generated:

1.2.1 Laser-ablation of a Metal Target

A Si-Fe target is ablated using a pulsed laser[2, 13]. From the equilibrium phase diagram for Fe-Si (see section 2.1), it can be seen that Fe-$Si_{(l)}$ and $Si_{(s)}$ coexist at $T > 1207\ ^{o}C$ and $\sim 90\%$ Si atoms. This gives the required composition for the target. The ablated target condenses into silicon-rich Si-$Fe_{(l)}$ nanoclusters, which supersaturate in Si, and precipitate it out as a nanowire. Growth continues as long as the wire remains in the heated region of the furnace (above 1200 °C). Since both Fe and Si atoms are being supplied, the wire diameter increases along its length. Pure crystalline nanowires with diameters from 6-20 nm and lengths exceeding 1 μm have been grown in this way.

The use of laser-ablation is critical because it results in a gas that condenses rapidly and is highly supercooled. Because of this supercooling, the liquid metal clusters can be nanometer-sized. If the supercooling did not occur (as in the case of a normal gas slowly condensing), then the minimum droplet size would be limited by equilibrium thermodynamics[3] to at least:

$$r_{min} = \frac{2\sigma_{LV} V_L}{RT \ln(\sigma)}$$

where σ_{LV} is the vapour-liquid surface free-energy, V_L is the molar volume and σ is the vapour supersaturation. This radius is of order 0.2 μm, and is far too large to yield interesting nanowires.

Another method is laser ablation of Au with gaseous SiH_4[2]. In this case, the target for ablation is pure gold, which forms the nanoclusters first; then gaseous SiH_4 is added as the reactant. The phase diagram (section 2.1) shows that Au-$Si_{(l)}$ and $Si_{(s)}$ coexist at 18% Si, and temperatures above 363 °C. This method also has the advantage of a much lower reaction temperature. The wires that resulted at temperatures between 373-500 °C had diameters as small as 3 nm.

1.2.2 Gold Nanoclusters Pre-formed by Precipitation

An oxidised silicon wafer is the substrate and is covered with a surfactant. Then Au nanoclusters suspended in solvent are deposited on the surface; they stick electrostatically to the surfactant, but do

[3]For the droplet to grow, the Gibbs free energy released by the chemical reaction (as the volume increases) must outweigh the energy needed to create new interfacial surface area. Thus large droplets are stable and grow; whereas small droplets shrink and disappear. Supercooling causes a larger free energy change ($\Delta G = \Delta H - T\Delta S$) and so permits smaller critical droplets.

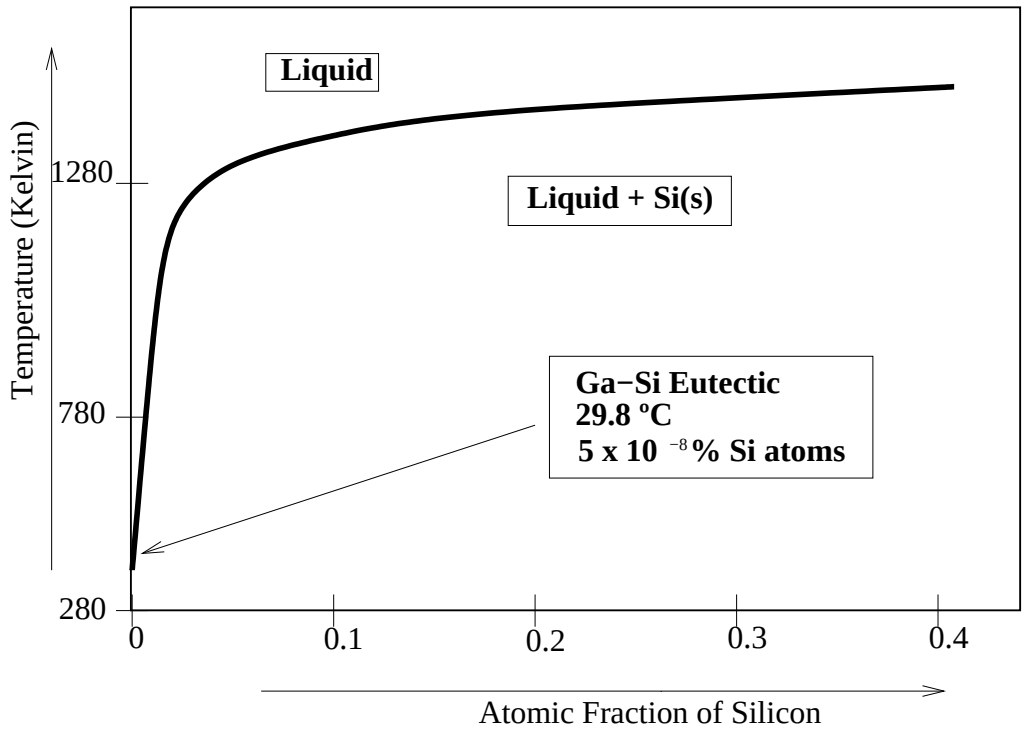


Figure 4: Ga-Si phase diagram, showing the Ga-Si eutectic with a very low Si content.

not coagulate[12]. This is then heated to 440 °C, and exposed to 10% SiH_4 in He. It results in wires of diameter 1-2 nm larger than the initial Au ball; thus the diameter may be accurately controlled. The Au balls used by Lieber et al. had diameters of 5, 10, 20 and 30 nm. These can either be produced by laser ablation of an Au target, as above, or they can be produced by precipitation of aqueous Au[34].

1.2.3 Low-temperature V-L-S Using Gallium

Using gallium, it is possible to synthesise nanowires at a low temperature, and without the need for nanometer-scale catalyst droplets. This is because, although Ga is very soluble in Si at high temperatures, it forms a Ga-Si eutectic with an extremely low Si content: only 5×10^{-8} at.%. This is shown in figure 4. There is the added advantage that this eutectic has a very low temperature of 29.8 °C[14].

Classical nucleation theory[15] for solute precipitation gives the critical diameter, d_c for a stable nucleus:

$$d_c = \frac{4\Omega\alpha}{RT \ln\left(\frac{C}{C_\infty}\right)}$$

where Ω is the molar volume, α is the surface free energy, and C and C_∞ are the actual and equilibrium concentrations respectively of Si in Ga. Since the equilibrium concentration of Si is so small, then nucleation is very strongly favoured, and the critical nucleus size for homogeneous nucleation is in the nanometer range: only 6 nm for 1% dissolved Si at 400 °C. The low miscibility and high surface-tension then cause the Si wires to surface out. Sunkara et al.[14] grew nanowires 6-50 nm in diameter,

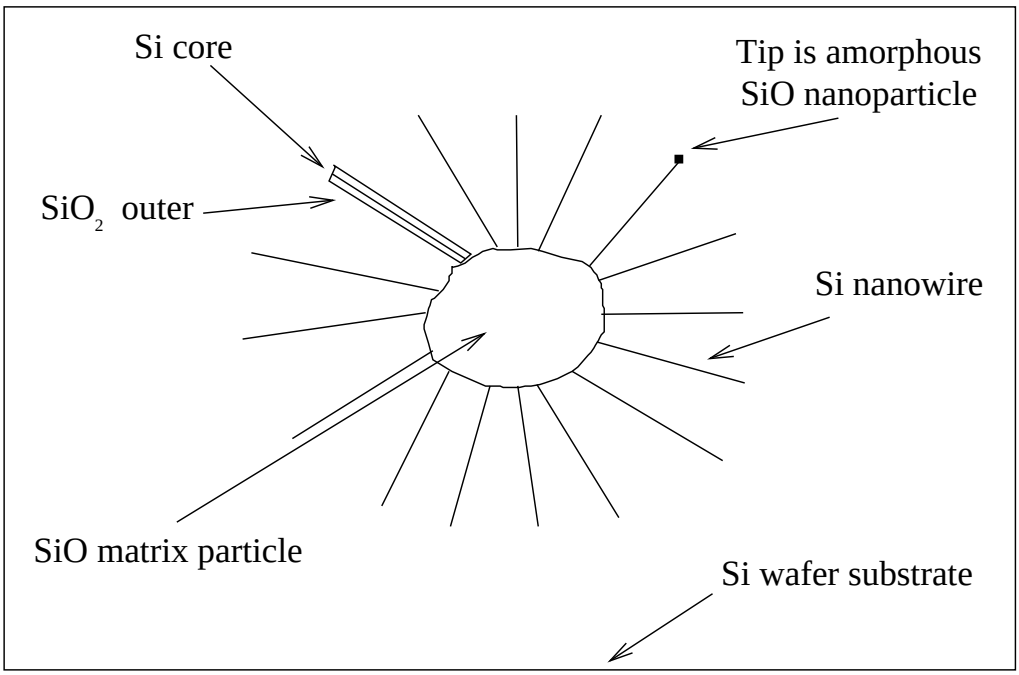


Figure 5: The typical morphology of nanowires formed by SiO disproportionation.

and hundreds of μm long by coating a Si substrate with Ga, and etching this in a 1:100 H_2:N_2 plasma at 700 W and 400 °C. The plasma reacts with exposed Si to produce $\bullet SiH_x$ radicals which are in turn decomposed by atomic hydrogen, catalysed by Ga:

$$\bullet SiH_{x(g)} \xrightarrow{\text{Ga}} \text{Ga-Si}_{(l)} + xH_{2(g)}$$

They found, as expected, that the wire length $\propto$ growth time.

1.2.4 Thermal Evaporation of SiO

This method[16] requires no metal catalyst, but does operate at a very high temperature. SiO powder is evaporated, and nanoparticles nucleate on the surface of the substrate. Then the SiO disproportionates:

$$2SiO_{(l)} \longrightarrow Si_{(s)} + SiO_{2(s)}$$

This process occurs at 950-1250 °C and forms nanowires with a Si core and an SiO_2 sheath. The sheath facilitates the 1-dimensional growth by confining the Si laterally, and keeping the molten SiO nanoparticle at the growth front, where it can easily absorb more Si-O.

Zhang et al.[16] obtained wires in this way of radius 10-100 nm and length 50 μm. The wires obtained at temperatures from 600-1350 °C had various morphologies: "tangled", "mushroom-like" or "hairy ball-like." The hairy ball morphology is shown in figure 5.

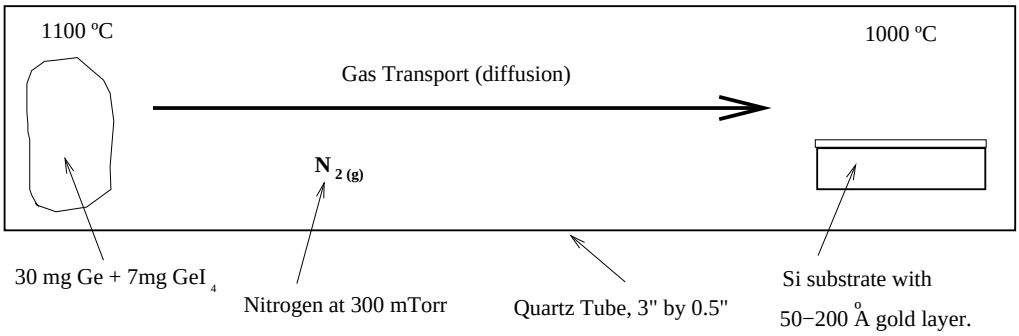


Figure 6: The reaction $Ge_{(s)} + GeI_{4(s)} \rightleftharpoons GeI_{2(g)}$ proceeds in the forward direction at the hot end of the tube, and the reverse direction at the cooler end, thus depositing Ge onto the Au layer.

1.2.5 Very Thin Gold Film

Wu and Yang[17] used a silicon substrate coated with an extremely thin layer (50-200 Å) of Au. This was placed at one end of a sealed tube, containing N_2 at a pressure of 30 mTorr, and a Ge/GeI_4 mixture placed at the other. It was then heated to 1100 °C. Germanium vapour was transported via diffusion, and nanowires grew on the substrate. The crystalline nanowires were found to be a few hundred μm long and 5-300 nm wide; the diameter reduced as the Au thickness was decreased. The experimental setup is shown in figure 6.

Wu and Yang used Germanium, which being larger than Si (with atomic Bohr radii of 24.3 nm and 4.9 nm respectively), shows quantum-confinement effects for wires five times larger. However, it is possible to adapt this method for silicon: the Au can be initially present as a very thin layer, rather than as laser-ablated nanoclusters. Westwater et al.[18, 1, 6] used this method with silicon, and patterned the Au onto the substrate; Teo and Bu used an uniform thin film of Au[35]. The film thicknesses are approximately 1 nm. The method of Teo and Bu produced a low yield as the reaction rate is limited by temperature. This motivates the use of plasma to enhance the reaction rate.

1.3 Summary of Reported Growth Conditions of Silicon Nanowires

Table 1 shows the process conditions published in the literature for growing Silicon nanowires, and reported as being successful. Various methods are summarised, grouped by catalyst metal. These include gold, zinc, nickel, iron, gallium, and uncatalysed silicon oxide.[4]

1.4 Comparison of Silicon Nanowire Growth Methods.

Of the methods above, the most promising seemed to be the laser-ablation of gold and low-temperature gallium methods; owing to the availability of facilities, the low temperature gallium process was favoured, and this was duly commenced. However, gallium is in Group III, and is also very volatile. It was therefore realised that the use of gallium would contaminate the equipment chambers used and that all subsequent samples would become doped p-type. Since these facilities are shared, this avenue of research had to be abandoned.

[4]Other semiconductor nanowires, such as Ge or InP are also promising. However, they are not included here.

Metal Catalyst	Process Gases used	Pressure (mTorr)	Temperature (°C)	Plasma	Result	Notes	Ref.
0.6 nm Au	40 sccm SiH_4 diluted to 10% in He	SiH_4 partial pressure: 0-1000	425-600	No	40-100 nm wide silicon nanowires	Low temperature produces kinked, or bendy wires. High temperature, low pressure produces fat, straight wires. See section 2.5	[18]
0.6 nm Au	40 sccm SiH_4 diluted to 10% in He	SiH_4 partial pressure: 0-1000	425-700	No	0-100 nm wide silicon nanowires	Localisation of wires obtained by etching holes in SiO_2 and Au sticks better to Si than SiO_2. SiH_4 produces much thinner wires than $SiCl_4$.	[1]
3 nm Au	40 sccm SiH_4 diluted to 10% in He	100	425-700	No	1 μm wide silicon nanowires	Wires grow precisely in the centre of Si islands, where the Au melts and agglomerates	[6]
5-30 nm Au nanoclusters	0-80 sccm SiH_4 diluted to 10% in He	100	440	No	7-32 nm wide silicon nanowires	Nanowire diameter is predictably ~ 2 nm larger than the initial Au ball.	[12]
0.5-1 nm Au (or Zn)	300 sccm He containing 5% SiH_4	100 000	450	No	5-25 nm wide silicon nanowires	Wires are straight, randomly oriented and sparse. Zinc also works as a low-temperature catalyst.	[19]
Au (1% Au +99% Si) - laser-ablated	50 sccm Ar	300 000	370-500	No	3 nm and wider silicon nanowires	Laser ablation used to form a vapour. This supercools and condenses to give nanoclusters. See section 1.2.1	[13]
Au thin film	80 sccm SiH_4	300	360	No	Low yield	a-Si:H recipe in DP80 system. The low yield is due to the low temperature available. Plasma is believed not to have been used.	[35]
10 nm Ni on a Si wafer	200 sccm Ar and 20 sccm H_2	7500	820	No	40 nm wide tangled silicon nanowires	The wires are grown directly from the Si wafer by vapour transport. O_2 contamination makes crystalline wires amorphous.	[20]
Ni (10% Ni +90% Si) - laser-ablated	50 sccm Ar	300 000	n/a	No	n/a	The laser ablation method also works for Ni.	[13]
Fe (5% Fe +95% Si powder)	150 sccm flow of Ar across the FeSi plate	150 000 - 600 000	1250	No	8-15 nm wide silicon nanowires	Wire diameter varies with pressure: $d \propto p^{0.4}$. The pressures are nearly atmospheric: much higher than for Au-Si.	[21]
Fe (10% Fe +90% Si) - laser-ablated	50 sccm Ar	300 000	>1200	No	6-20 nm wide silicon nanowires	Laser ablation used to form a vapour. This supercools and condenses to give nanoclusters. See section 1.2.1	[2, 13]
Ga "thin-film" on Si substrate	1:100 sccm H_2:N_2 plasma	n/a	<400	700W	6-50 nm silicon nanowires	Low temperature VLS. The smallness arises because Si is very insoluble in Ga.H_2 plasma etches the Si substrate. See section 1.2.3	[14]
SiO powder, no catalyst	n/a	n/a	950-1250	No	0-100 nm silicon nanowires	SiO is evaporated and disproportionates. The resulting wires have varied morphologies. See section 1.2.4	[16]
SiO powder	50 sccm Ar containing 5% H_2	400 000	1300	No	8-46 nm silicon nanowires	Very long, highly oriented, densely packed wires are produced. Ar is a carrier gas, H_2 etches the wires to improve their structure.	[22]

Table 1: The conditions reported in the literature for the growth of silicon nanowires. Some authors do not report their process conditions in full: these are denoted "n/a".

In view of the published literature, and the equipment available to the group, the method chosen was a hybrid. The principal conditions were the use of thin-film Au as the catalyst, and SiH_4 as the silicon source-gas. The reactions were at intermediate temperatures in the range 300-400 °C. Other thin-film metal catalysts (Fe, Co, Ni) were investigated, and Au nanoclusters (from Junfeng Geng) were also used. The reaction gas mixture was varied, mixing in He or H_2 and an RF-plasma was used to assist the SiH_4 dissociation reaction to compensate for the low temperature available. The nanowire growth took place in a Plasmatech DP80 Plasma Deposition System, which has an upper limit on temperature of 400 °C and an upper limit on pressure of approximately 1000 mTorr.

2 Theoretical Models and Processes

This section introduces the relevant theory, and explains the principles of operation of the RF-PECVD process used. It details the eutectic and silicide reaction mechanisms of the metal catalysts; the production of gold nanoclusters; the operation of the DP80 system; the competitive etching and deposition of amorphous and microcrystalline silicon; and the control of nanowire parameters via the growing conditions.

2.1 Metal Catalyst: Eutectic and Silicide Mechanisms

There are two mechanisms by which metals may catalyse silicon nanowire growth: the eutectic method, which is the case for gold,[2] and the silicide reaction, which is the case for iron,[2] cobalt, and nickel.

For the gold-catalysed methods, the phase diagram (figure 7) shows that gold and silicon are mutually soluble to form a eutectic mix. This occurs at a temperature of only 363 °C, far lower than the melting point of either pure element. The gold assists the decomposition of silyl radicals; as additional silicon atoms are absorbed, the mixture moves away from equilibrium. Thus it is thermodynamically favoured for the cluster to split into a mix of $(\text{Au-Si})_{(l)}$ and $\text{Si}_{(s)}$. Surface tension causes the Si atoms to migrate to the surface, so a pure silicon nanowire grows out of the molten "blob", leaving a nanocluster sphere on the end of the finished wire. In the experimental method used, the pressure is lowered to $\sim 1/1000^{th}$ atmosphere, and the films of gold metal are initially very thin. Both of these factors will lower the critical temperature slightly below 363 °C, which is fortunate, given the pressure limit at which the DP80 system operates.

For the silicide methods, including Fe-Si, in contrast to eutectic mixing, a chemical reaction occurs bonding the Fe and Si. This $FeSi_x$ liquid alloy co-exists with solid silicon, thus Si atoms can enter the cluster from the gas phase, react with Fe, then dissociate and leave via the solid phase[21]. See figure 8. The mechanism is otherwise similar to the eutectic method. Although the silicide method is most efficient at high temperature, when the $FeSi_x$ is liquid, because the iron actually bonds with the silicon it can also work when the $FeSi_x$ is solid: this requires diffusion to operate, and is therefore much slower.

In selecting a catalyst, gold was chosen as the most promising, due to its comparatively low temperature, and previous success[35]. Iron was selected, despite the disadvantages of remaining solid,

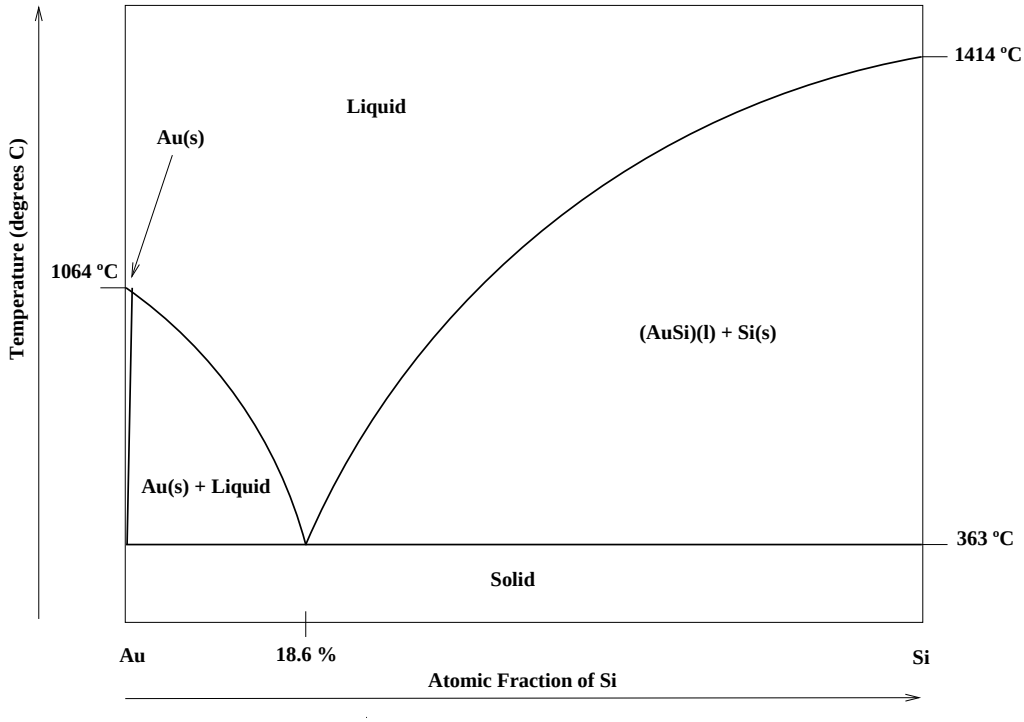


Figure 7: The equilibrium phase diagram for Au-Si at atmospheric pressure. This shows the eutectic melting point at 363 °C above which the VLS method can operate.

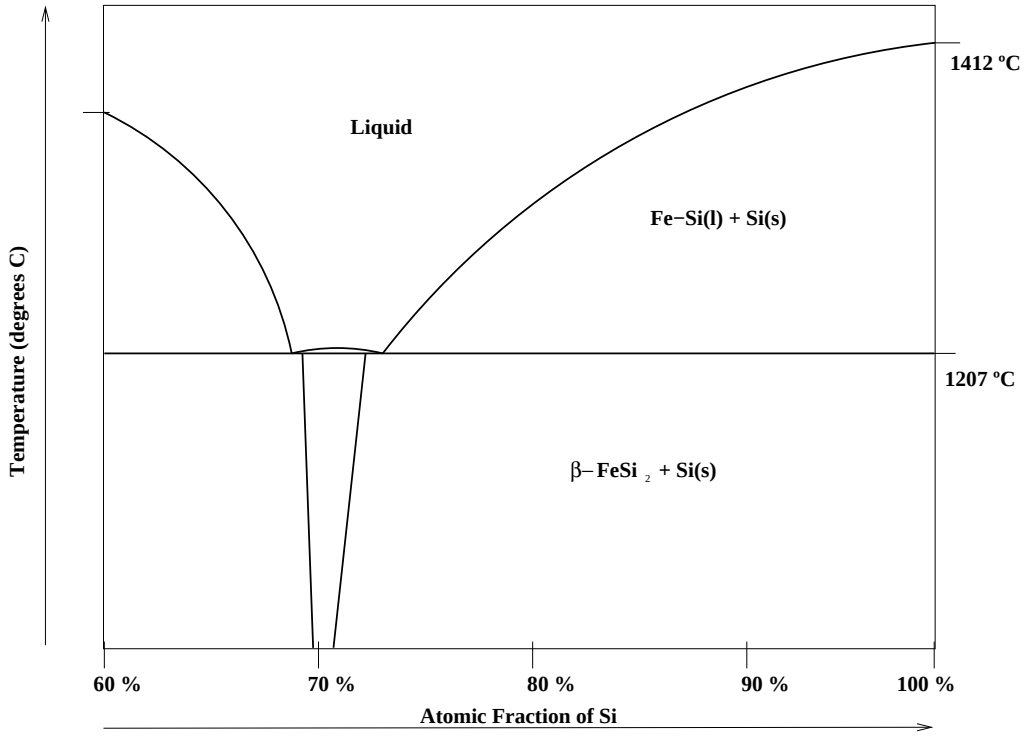


Figure 8: The equilibrium phase diagram for Fe-Si shows that temperatures greater than 1207 °C are required to form a liquid iron silicide.

limited by the rate of diffusion, and the potential for further difficulties due to oxidation, because of its great potential as a dual catalyst for both Si-nanowires and C-nanotubes. Nickel also requires high temperatures, but rather than mediating the reaction, it is itself consumed. Thus it has the potential to produce "nanocones", with very sharp tips[35]. In addition, one more transition metal catalyst was chosen: Cobalt.

2.2 Gold Nanoclusters

Small clusters of Au are needed to catalyse the nanowire growth, and it is necessary for the molten Au catalyst ball to supersaturate with Si. These small clusters of Au can be obtained in two different manners:

1. Thin films of Au, a few nm thick, will melt when heated and will form into droplets by surface tension. The thinner the film is, the smaller these droplets will be. The normal melting point of Au is 1065 °C, but this can be greatly decreased by the effects of film thinness. The Au layer is only a few tens of atoms across: this means that the surface free energy of the film is large in comparison to the bulk heat capacity, so the thermal energy that needs to be supplied for melting is much lower. Gold droplets can also form below the melting point by diffusion: this requires high temperatures (a significant fraction of the melting point), and longer times. The formation of droplets should ideally occur in the same process as the SiH_4 exposure, without pausing for a cool-heat cycle which might cause agglomeration. However, the DP80 system only reaches 400 °C, thus a separate step of manufacturing Au clusters in the furnace was sometimes also used: this is explained in section 3.3. Factors affecting droplet size and shape include film thickness, temperature and the contact angle between the molten Au and the SiO_2 substrate. The droplets have a low aspect ratio: their diameter is approximately 50 times the initial film thickness[23]. The smallest droplets are formed from the thinnest films annealed at the lowest temperatures (providing that the temperature is sufficient to permit diffusion), for the the shortest times.

2. Gold nanoparticles (obtained from Junfeng Geng) are precipitated by the reduction of Aqua Regia, $HAuCl_{4(aq)}$ by Citric Acid. The resulting colloidal Au suspension has clusters of Au with diameter 12 nm ± 10% and contains 0.01 g of Au per 100 ml H_2O[34]. These can be applied direct to the silicon substrate; the water is then allowed to evaporate.

Although the gold tends to break-up due to surface-tension at high temperature, the clusters will tend to agglomerate by diffusion at lower temperatures. Thus, as the samples slowly cool after the reaction process, the Au aggregates together. The DP80 system takes 3 hours to cool, so the finished sample is well annealed when it is unloaded. A further limitation of the DP80 is that during a single experimental process, the temperature may cool from 400 °C to 300 °C over the course of one hour, thus the deposition of any one experiment proceeds over a range of temperatures, and a range of cluster sizes.

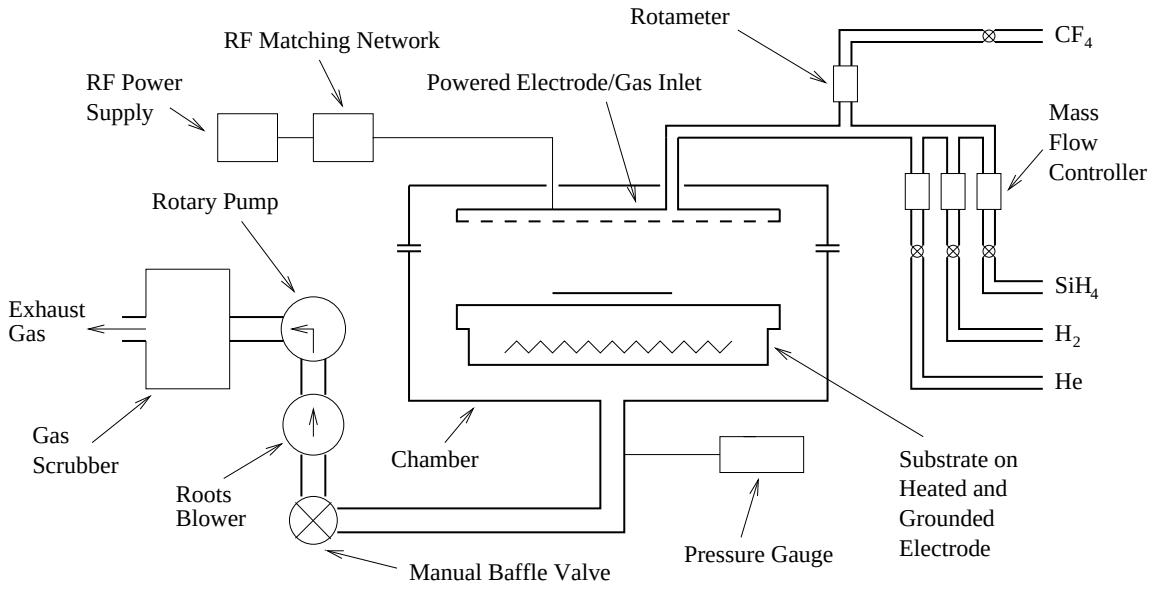


Figure 9: Simplified Schematic of the DP80 RF-PECVD system.

2.3 RF-Plasma-Enhanced Chemical Vapour Deposition

The nanowires were grown in a Plasmatech DP80 Chemical Vapour Deposition System, shown schematically in figure 9. This can operate at temperatures up to 400 °C, and pressures up to an absolute *maximum* of 2000 mTorr. Silane (SiH_4) gas is used, which can be optionally diluted with H_2 or He. The available flow rates of these gases are 100, 500 and 2000 sccm[5] respectively; the mass flow controllers can regulate these to within 1% of the maximum flow rate. The deposition may be assisted by striking plasma: the 13.56 MHz RF supply can provide up to 300 W.[6]

Chemical Vapour Deposition occurs when the source gas, SiH_4 decomposes thermally inside the heated chamber. The resulting radicals collide with the substrate, and the walls of the chamber. If they are not removed by the pumping system, they are deposited as a thin film. Deposition occurs preferentially on the substrate because the Si is absorbed into the molten Au catalyst. However, even at 400 °C, thermal decomposition of SiH_4, if it occurs at all, is very slow. Thus a plasma is used to enhance the process: the additional energy provided by the RF power supply ionises the gas, and forms a plasma. In consequence, the SiH_4 dissociation temperature is lowered, so Si ions and radicals are more reactive, and available in greater quantity. So deposition occurs at a far greater rate and the nanowire growth reaction can proceed at a far lower temperature than it otherwise would. However, the plasma also causes the ions, both Si and H to bombard the surface of the wires: this results in defects in the structure, as well as implanted hydrogen impurities. Further side-effects of the plasma are some additional heating of the substrate, and that an electric-field with a dc-bias is created inside the chamber. This encourages the wires to align parallel to the E-field, and stand up vertically. The standard "recipe" [33] for depositing a:Si-H in the DP80 is 80 sccm of undiluted SiH_4 at 300 mTorr and 300 °C with 6 W of RF power. The bond energy for Si-H bonds is 318 kJ/mol,

[5]Sccm is an abbreviation for "standard $cm^3$of gas flow per minute". (Standard conditions are atmospheric pressure at 0 °C.)

[6]Although the DP80 can be pre-heated to 400 °C, once the gas flow is commenced, it cools. Especially at high gas flow rates, the maximum temperature that can be maintained is approximately 320 °C.

so approximately 8% of the SiH_4 is dissociated. This deposits 10 nm of a-Si:H per minute, and was used at the maximum nominal temperature of 400 °C as the basis for the growth of silicon nanowires. The higher temperature is necessary to exceed the critical Au-Si eutectic temperature, as well as to increase the reaction rate.

2.4 Amorphous and Microcrystalline Silicon Growth

The silicon nanowires grown are single-crystal, although they sometimes have defects causing the growth directions to switch suddenly from one [111] direction to another[1]. Ideally, the wires should be grown thermally, using just high temperature, and no plasma. However, since SiH_4 is too stable to thermally decompose at the temperatures available in the DP80, plasma was introduced to aid the reaction; in consequence, amorphous silicon is deposited on the substrate even without the presence of any catalyst. This a-Si:H (amorphous silicon containing some extra hydrogen) is an undesirable side-effect: not only does it cover the substrate and contaminate the wires, but it can also "bury" the nanowires, covering them partially or completely.

By introducing hydrogen into the reaction gas mixture, such that the Silane is highly diluted, and increasing the plasma power greatly, it is possible to deposit microcrystalline silicon (μc-Si) on the substrate instead of a-Si:H. The presence of a majority of hydrogen also causes the a-Si:H to be etched away: with the (hopeful) result of leaving clean, highly crystalline nanowires. In addition to removing contamination and covering, use of the conditions for growth of microcrystalline/nanocrystalline silicon is expected to produce a nanowire that has properties resembling μc-Si. Compared to a-Si:H-like wires containing a significant fraction of hydrogen, it should be more stable over time, and have a higher carrier mobility[24].[7]

When hydrogen is added, there is a dynamic equilibrium between the competing processes of deposition and etching:[25, 26]

$$SiH_{4(g)} \rightleftharpoons Si{:}H_{x(s)} + (2 - \frac{x}{2})H_{2(plasma)}$$

This reaction is driven to the right, favouring deposition of a-Si:H by low plasma power, low pressure and high silane concentration. The reaction is driven to the left, favouring hydrogen-radical etching of a-Si:H, (but still permitting deposition of μc-Si) by large hydrogen dilution, high pressure, and high plasma power. The growth of both amorphous and microcrystalline films normally proceeds at a similar rate; however, in the presence of hydrogen radicals, caused by plasma, the amorphous silicon is removed at a far greater rate. This is because the crystal structure of amorphous silicon is under much greater strain due to defects; thus it is more readily attacked by hydrogen radicals than is microcrystalline silicon.

Heintze et al.[25] found that there is a point where amorphous silicon is etched and microcrystalline silicon is deposited: this occurs at a dilution of approximately 200:1 H_2:SiH_4. Their results for pressure of 150 mTorr, plasma power of 4 W and temperature of 200 °C are shown in figure 10 and summarised in table 2.

[7] Pure, bulk microcrystalline silicon has a carrier mobility up to 1000 times greater than hydrogenated amorphous silicon. This indicates that crystalline, hydrogen-free nanowires are desirable.

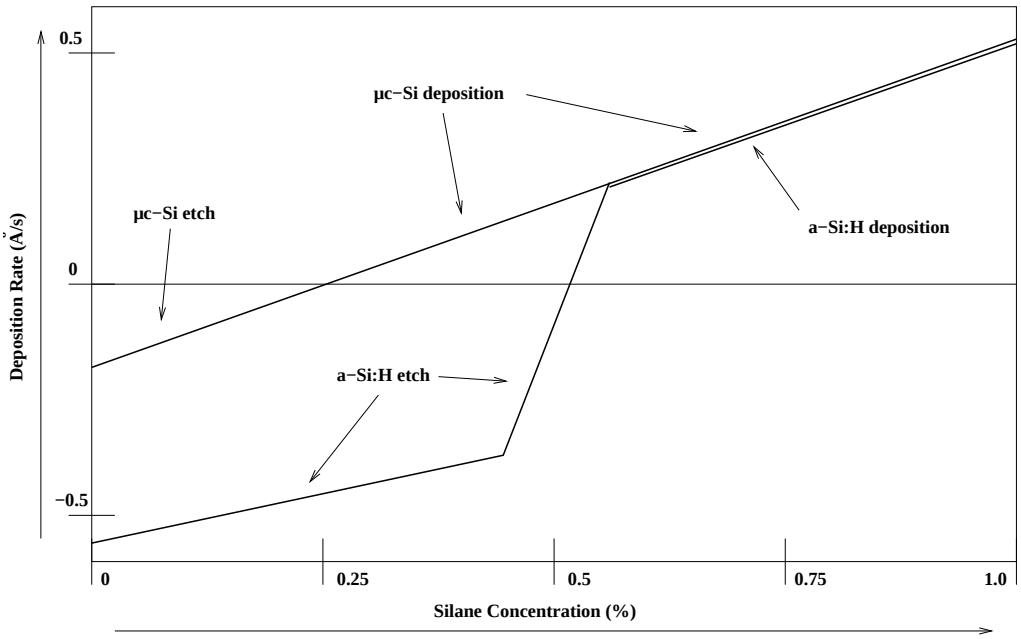


Figure 10: As the silane concentration falls, both amorphous and microcrystalline silicon are progressively deposited less and etched faster. However at a ratio of 200:1 H_2:SiH_4, the amorphous silicon suddenly switches from deposition to etching.

Silane fraction in Hydrogen	**Consequence**
< 0.25 %	Both amorphous silicon (a-Si:H) and microcrystalline silicon (μc-Si) are etched away.
$0.25\% < x < 0.45\%$	a-Si:H is etched away, but μc-Si is deposited
$> 0.45\%$	Both a-Si:H and μc-Si are deposited

Table 2: Deposition and etching of amorphous and microcrystalline silicon[25].

It is hypothesised that hydrogen dilution ratios between 2:1 and 20:1 should be investigated in addition to the use of pure SiH_4 and SiH_4 in He as an inert buffer gas[36]. The purpose is not to grow microcrystalline silicon outright; rather it is to etch away some of the contaminating amorphous silicon which, as a consequence of the need for plasma, contaminates and masks the wires. However an alternative hypothesis due to Andrew Flewitt[37] states that the presence of the Au catalyst will enhance the forward reaction, and that there may be a narrow, optimal window at dilution rates above 100:1. In such a region, etching would normally dominate totally, however the Au might overcome it locally. If this were correct, it would yield nanowires of very high quality, although locating that region might prove elusive.

The "recipe" [37, 26] for depositing μc:Si-H in the DP80 is 10 sccm of SiH_4 diluted between 1:5 and 1:100 with H_2 at 100-500 mTorr and 250 °C with 200-300 W of RF power.

2.5 Control of Nanowire Parameters via Growth Conditions

The conditions under which the nanowires are grown affect their properties. The following explains what is expected to occur and the reasons for it.

- Since the catalyst is not used up, and the nanowire remains fixed in the heated zone, it is expected that the growth reaction will occur at a constant rate, yielding nanowires whose length is proportional to the reaction time, assuming a constant process temperature. This is widely reported to be the case.
- The Gibbs-Thomson equation gives the critical diameter for nanowire growth, thus placing a minimum limit on the size of wires that can be grown under given conditions of temperature and pressure. Equilibrium thermodynamics gives the critical diameter, d_c in terms of the surface energy for the solid/vapour interface, γ_{sv} , the molar volume of silicon, Ω and the molar free energy change of solidification from the gas, $\Delta G_{s,m}$:

$$d_c = \frac{4\gamma_{sv}\Omega}{\Delta G_{s,m}}$$

  In terms of the standard molar Gibbs free energy change for sublimation, $\Delta G^{\circ}_{sub,m}$ this becomes:

$$d_c = \frac{4\gamma_{sv}\Omega}{-\Delta G^{\circ}_{sub,m} + RT\ln p}$$

  This shows that the smallest nanowires require high pressures and low temperatures. This has been found to be the case by Westwater et al.[18] who experimented between 320 - 600 °C and between 10 - 1000 mTorr: their summary is reproduced in figure 11 and shows the following behaviour:

  - Increasing the temperature at a constant pressure causes the wires to become thicker. Also, the reaction will be faster, causing speedier growth. However, the effect of higher temperatures cannot be investigated in this thesis.

  - Increasing the pressure at a given temperature first causes the wires to become thinner. After this, they then tend to become kinked, due to growth instabilities at the liquid/solid interface[27].
  - At high pressure (1 Torr), and low temperature (320 °C), the wires are at their thinnest, but the kinking has become extreme: the wires are highly curved and turn randomly.

- High pressure is favoured for growing high quality nanowires. However a low silane concentration is also desirable in order to slow the growth rate, causing better quality crystals containing fewer defects to grow. This may be achieved by diluting the SiH_4 in He. A 10% silane fraction is reported in much of the literature, which gives a good trade-off between growth rate and defect removal. This works because He atoms impact the growing surface of the wire. Si atoms which are bound less securely if they are in a defect such as a proto-dislocation are thereby either knocked back into the perfect position, or removed entirely from the growing point. A further advantage of He is that it assists in transferring the energy from the RF plasma to the silane.

- In the case where the liquid droplets are formed by condensation from gas (laser-ablation of or hot argon flow over an Si-Fe plate), then at low pressures, the size of the cluster, and hence the nanowire is expected to obey the inertia fluid model due to Yoshida et al:[28] $d_m \propto p^n$ where d_m is the diameter of an ultrafine particle, p is the pressure, and $n = \frac{1}{3}$. Zhang et al.[21] measured a value of $n = 0.4$. However, if the droplet size is predetermined, then the nanowires should be 1-2 nm larger than that size[12]. Thus in the case of Junfeng Geng's 12 nm gold 'balls', nanowires of about 14 nm diameter are expected. In the case of the thin metallic films, the temperature will determine how they melt and shape into clusters, so that thicker layers of metal result in thicker nanowires.

- Because of the Gibbs-Thomson condition, the nanowires should be thinnest at low temperature. However if the pressure exceeds 1 atmosphere, the sign of the contribution due to temperature changes: smaller nanowires are then favoured by higher temperature. In any case, it is necessary to have sufficient energy to dissociate the silane, and to obtain a reaction that is fast enough to be practical.

- The use of SiH_4 is capable of producing far thinner wires than can be grown by the decomposition of $SiCl_4$. Because silane is much more unstable, its bulk reduction by hydrogen is thermodynamically possible at all temperatures, whereas $SiCl_4$ can only be reduced at high temperature. In the case of wire growth, only SiH_4 has the scope to offset the increase in wire surface energy while maintaining an overall negative Gibbs free-energy change, $\Delta G \leq 0$.

- The use of plasma is expected to decrease the quality of the nanowires, since it encourages hydrogenated amorphous silicon. However, although Teo and Bu[35] grew some wires without the aid of plasma, the yield was very small. Therefore, because of the low temperatures available, the use of plasma is likely to be necessary to obtain sufficient decomposition of silane..

- The wires tend to grow in the [111] crystallographic direction[13, 2]. However, a wire may suddenly switch at random between this and another {111} direction forming a sharp kink: this is especially common at low temperature[1].

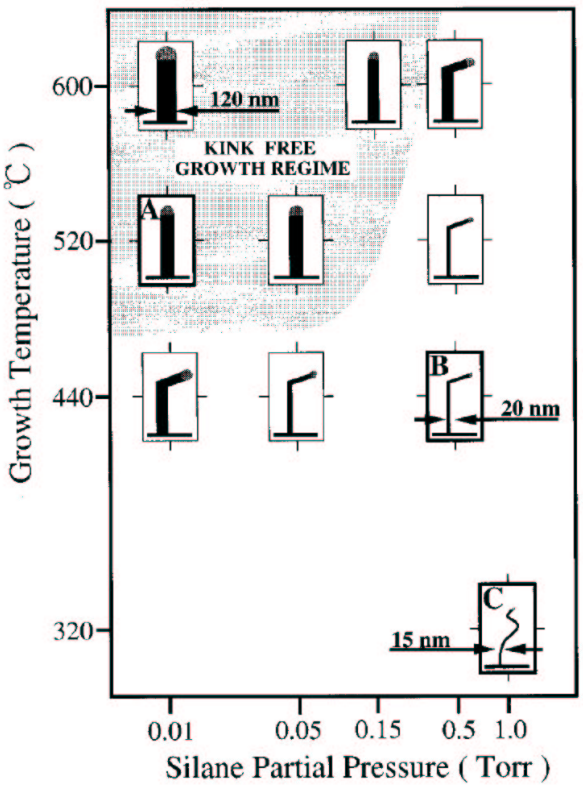


Figure 11: The dependence of wire morphology and width on the growth temperature and pressure. This diagram does not show the effect of reaction time, and is due to Westwater et al.[18]

- If plasma is used, then the DC component of the electric field within the DP80 should encourage the wires to stand vertically, and align. However whether this occurs depends on the field strength. Also long wires without a tendency to kink are most likely to be influenced by an electric field. Otherwise, the wires are expected to form a tangle of "spaghetti". Chhowalla et al.[23] report that electric field strengths of 0, 0.07, and 0.15 V/μm cause no alignment, partial alignment and full alignment of the wires. The dc-bias of the plasma in the DP80 system[8] when running at 6 W is approximately 0.01 V/μm[37] so alignment is not expected.

3 Growth and Analysis of Silicon Nanowires

The experimental techniques used to grow silicon nanowires are now presented. The precise conditions were varied, however the basic process was always the same: a substrate was coated with the metal catalyst, processed in the DP80 deposition system, and then examined in the optical and electron microscopes.

[8]The DP80 has circular plates 22 cm diameter and 4 cm apart. The plasma sheath is 4 mm wide, and has an estimated average bias of 50 V positive with respect to the ground electrode.

3.1 Silicon Substrate

100 mm diameter <100> oriented silicon wafers were used. These were 525 μm thick, and polished on one side. n++ silicon (heavily doped with antimony and with a resistivity of 0.015-0.025 Ωcm) was selected because it is highly conductive: this is in order to aid charge dissipation in the electron microscope. A layer of oxide was formed on the silicon in order to create a diffusion barrier to prevent the thin layer of metal from diffusing away from the surface into the substrate. The wafers were placed in a furnace at 1000 °C[9] for 40 minutes under a 4 dm^3/minute flow of oxygen; the furnace was then allowed to cool while the oxygen flow was maintained. This formed a hard layer of SiO_2 approximately 90 nm thick,[10] and the originally grey wafer appeared a deep metallic purple in colour. This oxide layer provided an excellent diffusion barrier. Potential difficulties with this insulation causing charge build-up in the electron microscope were avoided because of the subsequent metal coating. To avoid the risk of cracking the subsequent thin metal coating off the surface, the wafers were now cleaved into smaller (approximately 3 cm x 3 cm) pieces for subsequent processing. Some 25 mm amorphous quartz discs (Spectrosil type B) were also used as substrates: these allow for Raman (and UV-Visible) spectroscopy for analysis.

3.2 Evaporation of the Metal Catalyst

The Si pieces were then coated with a thin layer (between 0.5-5 nm) of metal catalyst, usually Au, but also Fe, Co or Ni. An Edwards Evaporator was used, operating at a pressure of 10^{-6} mbar and the metal was placed in an electrically heated "boat". The wire used was 99.99% purity 0.5 mm diameter gold. Raman spectroscopy later showed that this contains some carbon as an impurity. To evaporate gold, lengths of $\frac{1}{2}$,1,3 and 5 mm were used, to give thicknesses of approximately $\frac{1}{2}$,1,3 and 5 nm of coating. The gold was heated in a 25 Amp molybdenum boat for 3 minutes, whereas the other metals required 60 Amps in a tungsten boat to reach the higher temperature needed. The metals normally boil at temperatures of 2807, 2750, 2870 and 2732 °C for Au, Fe, Co and Ni respectively. However, because the vacuum pressure is only 10^{-6} mbar, such high temperatures are not required: it is only necessary to exceed the vapour pressure of the metals at this point, requiring temperatures of 942, 1002, 1055 and 1052 °C respectively[29].

In later experiments, the gold was applied via a shadow-mask in order to pattern it, and control the location of the nanowires. This shadow mask was either the usual type with alternate 1.0, 0.7 and 0.5 mm holes, or in some cases, a very fine "1000 mesh" Au TEM grid.[11] The TEM grid is a mesh of very fine gold wires: this was used as a mask, and then itself loaded into the deposition system with

[9] The furnace is set to 800 °C to obtain an actual temperature of 1000 °C.

[10] This thickness is not critical, provided it prevents the metal catalyst "disappearing" into the substrate. Westwater et al.[6] use an oxide layer 100 nm thick; Yu et al.[19] use a 150 nm barrier. The actual thickness was measured using an ellipsometer.

[11] The gold mesh TEM grid is designed for transmission electron microscopy, with the aim of growing wires supported only at the ends, and without having a solid backing. it is also useful for scanning electron microscopy, as it should permit better images to be obtained, and reduce the density of tangled nanowires. To use it as a shadow-mask, it may either be held in place by an ingenious patent-pending method,[38] or taped *carefully* onto the sample with vacuum tape. The latter method may destroy the (expensive) grid. It is important to keep the grid flat against the sample to ensure the Au pattern is in focus. The grid itself is circular and 3 mm in diameter; it contains 5 μm gold wires on a rectangular grid with a pitch of 25 μm.

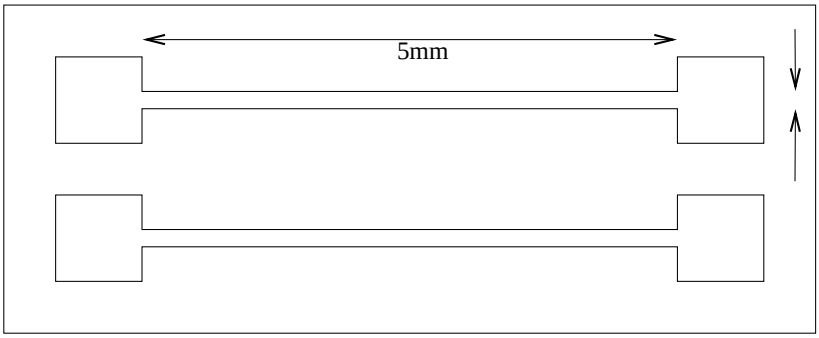


Figure 12: The shadow mask for measuring metal thickness. This mask was placed over a glass slide and loaded onto the sample stage in the evaporator. The resistance could then be measured using a multimeter, and the thickness calculated using $R = \frac{\rho l}{A}$ For example, a measured resistance of 102 Ω gives a thickness of 4.34 nm. Note that this technique tends to overestimate the resistance, and underestimate the thickness for the following reasons: the contacts have resistance (they are points and the current must spread out through an annulus); the probes scratch away the gold; and the glass surface is not flat (so the path length is longer than it ought to be and there are islands of Au which carry no current at all).

the aim of growing wires in the empty space between the wires, so that better SEM images could be obtained.

The resulting coatings are shiny but not opaque; they are also very soft and can easily be wiped off. The thickness can be either calculated or measured: both methods agree to within the variation across the sample stage. To calculate the thickness, it was assumed that the initial volume of metal in the boat was uniformly distributed over a hemisphere of radius r. For a wire of length l and diameter d, the thickness t of the coating is given by:

$$2\pi r^2 t = \frac{\pi d^2 l}{4}$$

Since the evaporator has a radius of $r = 15$ cm, the thickness in nm is related to the length in mm by:

$$t \text{ (nm)} \approx \frac{9}{5} l \text{ (mm)}$$

There are also some losses as Au diffuses into the material of the boat, or collides with remaining air molecules. Using a shadow mask, as shown in figure 12, the thickness, t could be measured electrically using the known resistivity of Au. Although it was difficult to make contact to the thinnest films, this showed t (nm) $\approx 4.5l$ (mm), confirming the above calculation. However, samples are mounted on a horizontal stage within the evaporator and so both r and the angle of incidence, θ vary across the stage as shown in figure 13: $t \propto \frac{\cos^3\theta}{h^2}$ These variations may reach a factor of 2 for samples placed far from the centre of the stage. Thus the deposited thickness, t in nm is related to the length of wire l in mm which is evaporated by:

$$t(\text{nm}) \sim l(\text{mm})$$

3.3 Gold Nanoclusters

In most cases, the thin film of Au (or other metal) was not treated further before loading into the DP80. As discussed in section 2.2, when the film is heated, surface tension naturally causes it to

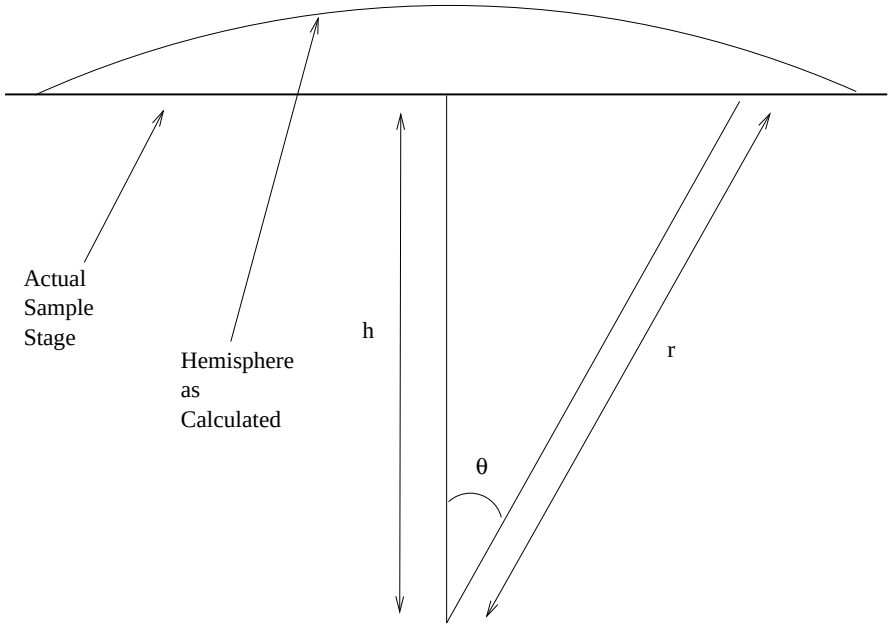


Figure 13: The evaporated thickness is not uniform. h is constant, but as θ varies across the stage, the source-distance, r increases, and the angle of incidence of the flux, θ becomes shallower. Thus $t \propto \frac{\cos^3\theta}{h^2}$. This can lead to variations as large as a factor of 2 between "identically prepared" samples. The actual values are: $h = 12$ cm, $r \leq 15.6$ cm and $\theta \leq 39$ °

break into small droplets. However, alternatives were investigated: either by pre-heating the gold layer in the furnace, or using colloidal gold nanoclusters supplied by Junfeng Geng.

3.3.1 Manufacture of Gold Clusters in the Furnace

Silicon substrates, coated with a 90 nm oxide layer, and then a layer of gold 1, 3, or 5 nm thick were placed in a furnace in order to form droplets. The furnace was preheated to either 300 or 500 °C and filled with nitrogen. The samples were then loaded into the furnace; after 5 minutes it was allowed to cool back to room temperature while the N_2 flow was maintained. Cooling took approximately 1 hour, thus the samples were annealed, not quenched. The initially shiny gold, red, or purple films turned dull, indicating that the film had become rough. The results of this are discussed in section 4.1.

3.3.2 Application of Colloidal Gold

The colloidal gold (supplied by Junfeng Geng) was applied to the silicon oxide surface by transferring droplets on the end of a thin steel wire, and allowing the water to evaporate. To vary the density of the gold balls, different areas of the substrate were given 1,5,10,15,20 and 30 applications. The use of a surfactant, poly-(L-lysine) or amino-silane, upon a roughened surface was considered in order to electrostatically stick the balls down and prevent agglomeration; however, early results showed that the colloidal gold was less effective than the flat thin films, so this was not pursued.

3.4 DP80 RF-PECVD

The samples were then loaded into the DP80 plasma deposition system. Typically, between 10 and 20 samples, after having had different treatments, were loaded at the same time to undergo the deposition. Samples were heated to 400 ^{o}C under vacuum and allowed to outgas for 3 hours. Then the process gases (a mix of SiH_4, H_2 and He) were admitted at various flow rates.[12] The gas flow was maintained for between 15 and 90 minutes and pressures between 300 and 1800 mTorr.[13] 6 W of RF power was supplied to create the plasma, except when a purely thermal reaction was desired. Finally, the samples were allowed to cool under vacuum before removal and cleaning of the chamber. The Au films were inert, and did not need cleaning before deposition. However, in the case of Fe, any oxide layer needed to be removed: this was accomplished immediately before the deposition by flowing 100 sccm of H_2 gas across the surface for 5 minutes to reduce the Fe back to pure metal.

3.5 Analysis

The resulting specimens were then observed by the following methods:

1. Visual Inspection to determine whether any reaction had occurred, and if so whether the surface was shiny and mirror-like (indicating a thick amorphous silicon film) or darker and dull, indicating the possible presence of nanowires.

2. Optical microscopy: using a high powered light microscope, with better than 1 micron resolution, very small objects could be seen. Because nanowires are crystalline and reflective, if large nanowires were present in quantity, they could be seen directly as bright hair-like objects.

3. Scanning Electron microscopy. The best of the samples were then observed in a JEOL Scanning Electron Microscope (SEM) (with assistance from Stephan Hofmann) using 5 keV electrons at a magnification of 50 000 and resolution of 5 nm. This allowed the wires, where they were present, to be seen in detail, and their lengths measured.

4. Raman spectroscopy. With the assistance of Andrea Ferrari, some of the samples were analysed by Raman spectroscopy. This is capable of analysing the degree of crystallinity of the wires.

3.6 Variations

The technique for processing and growth is explained above. Many permutations of pre-treatments and PECVD processes were investigated. Owing to practical limitations and the huge number of possibilities, not every combination was examined: for example, once it became apparent that metals

[12] Note that silane is pyrophoric - it is explosive on contact with air and without an ignition source. Caution needs to be observed.

[13] Note that the DP80 has an *absolute maximum* pressure rating of 2000 mTorr. This is not the limit in itself; rather it is when the pressure gauge goes off-scale. Pressures above 2000 mTorr cannot be distinguished from pressures which might exceed 1 atmosphere and could potentially force off the lid, releasing silane. Furthermore, it becomes difficult to operate the manual baffle valve with fine control above 1000 mTorr. Therefore 1000 mTorr is considered as the maximum standard operating pressure.

other than gold would not work at the limited temperatures available, this variable was removed from consideration. This optimisation was continued, always discarding the less successful ideas, and following the most promising. At all times, control samples of uncoated Si/SiO_2 were included. The following were investigated:

- Initial experiments with the a-Si "standard recipe" and without plasma showed no noticeable change to the samples. Subsequently the use of 6W plasma for 15 minutes on gold showed more promise, and motivated increased growth time.
- Different metals (Au, Co, Fe,) at 5 nm were tested. Also thin film (1 nm) gold and the gold balls from Junfeng Geng. The conditions were 400 °C, 300 mTorr, 80 sccm SiH_4 at 6 W plasma and a run time of 30 minutes.
- The above was repeated, but with the addition of 400 sccm of H_2 and the increase of pressure to 1800 mTorr (so as to keep the silane partial pressure the same). Many samples were loaded: 5 nm Au,Fe, Co, 15 nm Ni, 1 nm thin Au, Au balls (J.Geng), a gold TEM grid, and all four combinations of 5/1 nm Au pre-treated in the furnace at 300/500 °C. After this, it was concluded that the metals other than Au were not successful, and to concentrate on Au. Furthermore, severe cooling of the chamber showed that the gas flow had to be limited.
- The six combinations of 5/1 nm gold, either untreated, or pre-treated in the furnace at 300/500 °C. Also more Au balls (J.Geng) and some Au dots. These were treated at 400 °C, 1000 mTorr and a 1:10 dilution of SiH_4 in He (8 sccm, 72 sccm flow respectively). 6 W of plasma were used for 30 minutes. This was, however, not successful, yielding no nanowires.
- Gold films 1, 3, 5 nm thick and also gold balls. These were treated at 400 °C, 1000 mTorr, 80 sccm of undiluted SiH_4 with 6 W of plasma for 30 minutes. Some wires were found, but short, and fat suggesting an increase in run-time and decrease in Au thickness would be appropriate.
- 1:10 Hydrogen dilution was tested again, this time without plasma. Gold films 1, 3, 5 nm thick were used, either untreated, or pre-treated in the furnace at 300/500 °C. The conditions were: 400 °C, 1000 mTorr and a 1:10 dilution of SiH_4 in H_2 (8 sccm, 72 sccm flow respectively). The reaction was run for 30 minutes without plasma. This was a total failure: there was nothing at all.
- An attempt was made to repeat the above, with 1:50 hydrogen dilution and plasma. The conditions were: 400 °C, 1000 mTorr and a 1:50 dilution of SiH_4 in H_2 (2 sccm, 100 sccm flow respectively). 200 W of plasma were applied. This was intended to run for 30 minutes, but dwindling hydrogen forced termination after 5 minutes. Nevertheless, it was clear that nothing had reacted, and at this stage, it was decided to concentrate on pure silane.
- The thin films of Au (1, 3, 5 nm thick), gold balls, 2 nm gold patterned using a TEM grid, and the TEM grid itself were run at 400 °C, 1200 mTorr and 80 sccm of pure SiH_4. 6 W of plasma were applied for 1 hour. This showed a great deal of promise, although the wires were still too thick. It motivated an increase in pressure and time, and a decrease in thickness for the final experiment.

- $\frac{1}{2}$, 1, 3, 5 nm films of Au were used. The $\frac{1}{2}$ nm gold was also patterned using the TEM grid shadow-mask which was itself also loaded into the chamber. The final conditions were: 400 °C, 1500 mTorr, 80 sccm of pure SiH_4 and 6 W of plasma for 90 minutes. This yielded successful wires!

The individual results of each experiment are discussed in greater detail below, and also in the respective figure captions. Conditions of pressure, gas flow, and plasma power were monitored throughout the experiment, and maintained constant to within better than 2 % of their stated values. However, the temperature was only nominally 400 °C: it dropped during the course of the process, ending in the region of 320-370 °C, depending on the reaction length and the gas flow rate.

4 Results

The results of the experiments are now discussed. Optical and electron microscopy were used to view the samples: contrary to expectations, the better nanowire specimens were visible in the optical microscope. Raman spectroscopy was also attempted to characterise the crystallinity of the samples, but proved inconclusive. It was also possible, as experience was gained, to reject unsuccessful samples by visual inspection.

4.1 Manufacture of Gold Clusters in the Furnace

The gold clusters formed in the furnace were examined in the optical and electron microscopes. As expected, the clusters formed at lower temperatures were smaller on average, although there is a large variation. The thickest (5 nm) gold films clearly show droplet formation in the optical microscope; the 1 nm films appear almost smooth although their surface is dulled: this indicates that the smallest droplets are formed from thin gold layers heated to 300 °C. Figure 15 shows a 5 nm film heated to 300 °C; figure 16 shows a similar film heated to 500 °C. The droplets range up to 500 and 800 μm in diameter respectively. Figure 14 shows the 5 nm Au treated in the furnace at 500 °C and viewed in the SEM. This sample was also processed in the DP80 without plasma so it shows what happens to the gold once it has endured a further heat-cool cycle. The gold forms hexagons 300-800 nm in size; the fact that the edges are straight with sharp bends indicates that they are crystals (as they should be).

Thus it is possible to pre-form the gold droplets in the furnace, although they are an order of magnitude larger than the colloidal gold nanoclusters made by precipitation. Furthermore, the resulting products do not produce nanowires as good as those from the un-annealed films. Therefore this approach was not continued. The droplets formed in the DP80 from un-annealed films did have diameters of approximately 50 times their thickness, confirming the results found by Chhowalla et al.[23]

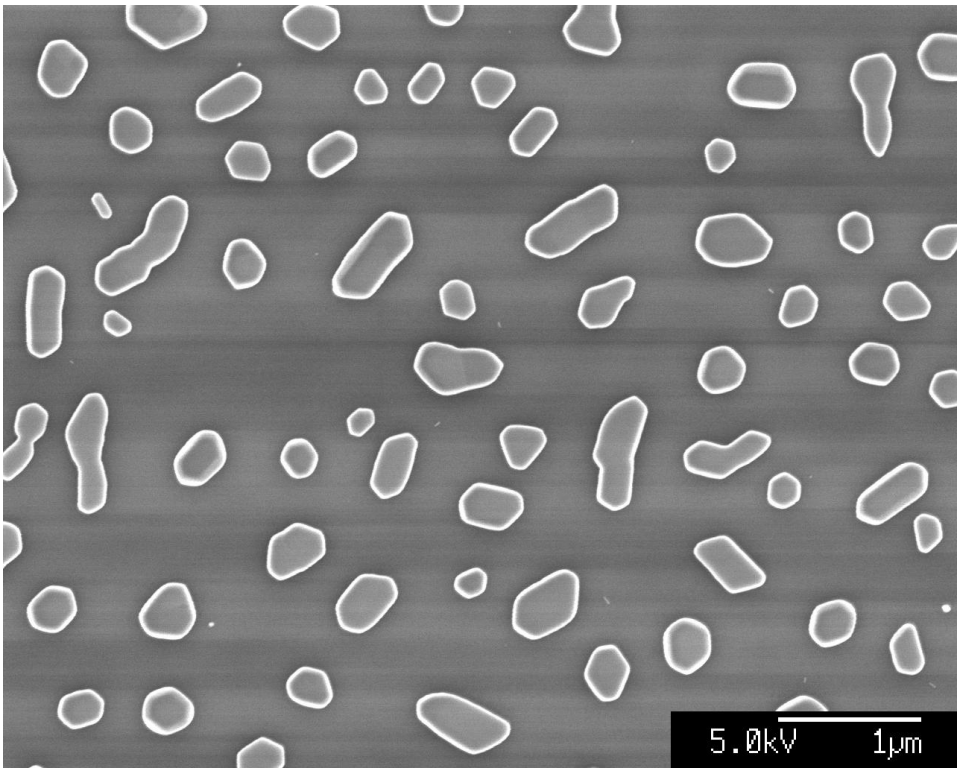


Figure 14: 5 nm Au, pre-treated in the furnace at 500 °C. The gold forms hexagons 300-800 nm in size. This image is from the electron microscope.

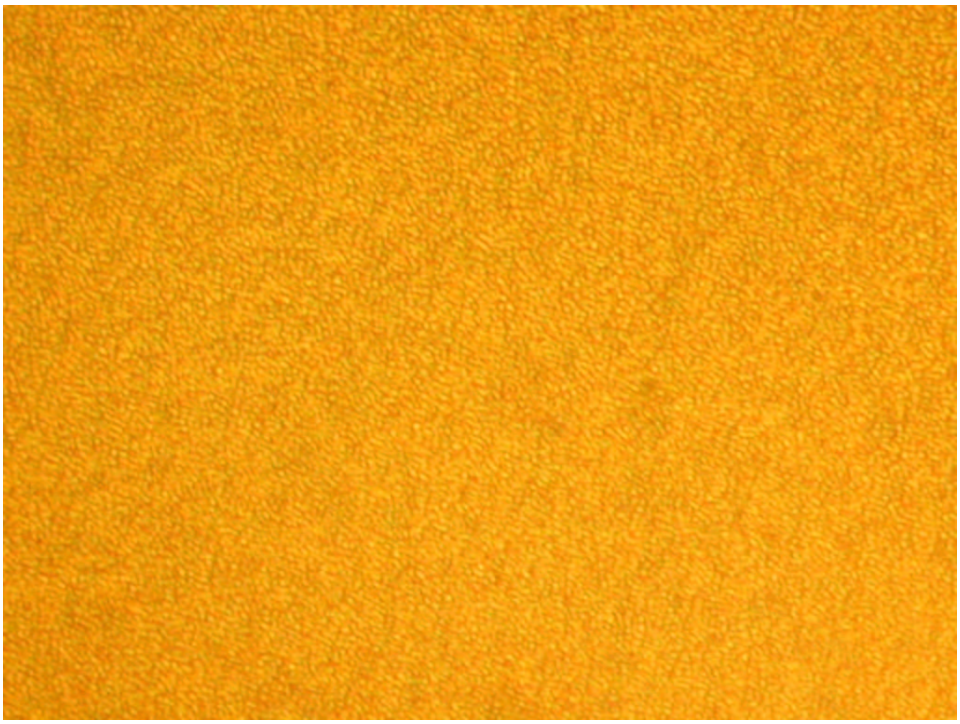


Figure 15: 5 nm Au heated in the furnace to 300 °C and then slowly cooled. The droplets range up to 500 nm in size. This image from the optical microscope is 100 μm across.

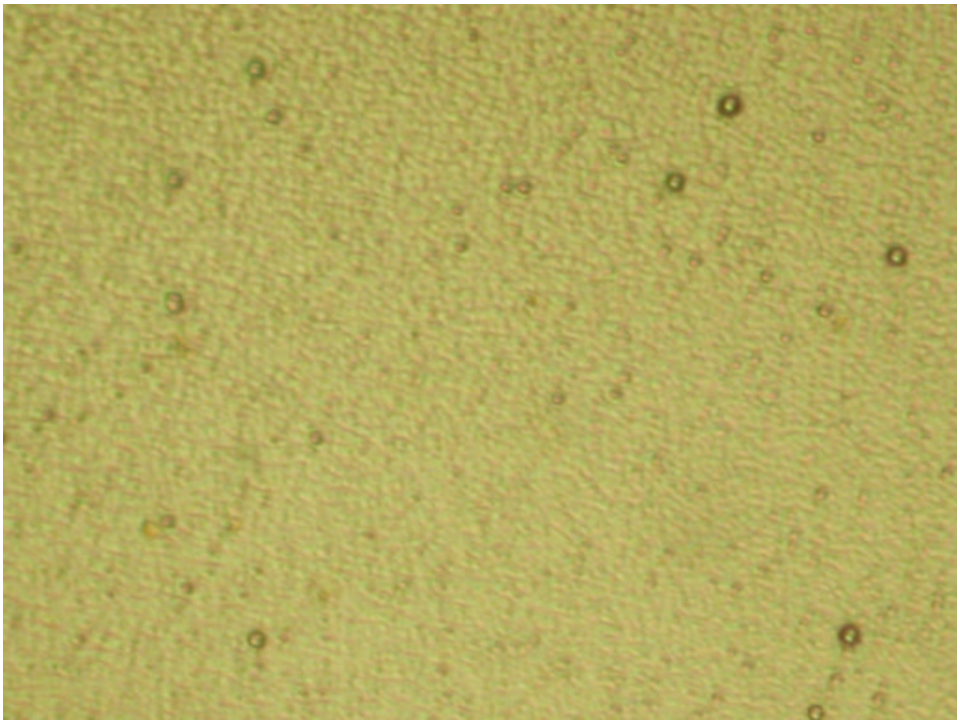


Figure 16: 5 nm Au heated in the furnace to 500 °C and then slowly cooled. The droplets range up to 800 nm in size. This image from the optical microscope is 100 μm across.

4.2 Growth of Silicon Nanowires.

4.2.1 Optical Microscopy

Before examining samples in the SEM, they were first examined by eye and in the optical microscope. Any sample that appeared shiny could be immediately rejected as being either unaltered or covered in amorphous silicon. Promising samples were darkened and unreflective due to scattering by the roughened, nanowire-covered surface; see Appendix C for more details. An example of an amorphous silicon covered sample is shown in figure 17: this is so thickly covered that the shiny a-Si layer has de-laminated and the sample appears cratered. It is also possible to see nanowires in the optical microscope: this has a resolution of 1 μm and an extremely small depth of field at high magnification. Because of this, it is easy to miss the nanowires (see figure 18), but it is also possible to see clearly that they stand up from the surface. Figures 19 and 20 show densely and sparsely packed nanowires respectively; it is clear in the latter that they are vertically aligned. All of these were processed in the same run under conditions of 400 °C and 300 mTorr with 80 sccm of pure silane, 6 W of plasma and a run-time of 30 minutes. The combination of inspection and optical microscopy was sufficient evidence to abandon investigation of metals other than gold, and hydrogen-dilution of the silane.

4.2.2 Scanning Electron Microscopy

Some of the many Scanning Electron Micrographs (imaged with the assistance of Stephan Hofmann) are now presented and the implications of each one are discussed. Where measurements are given, they are taken from the micrograph that allows the best measurement, whereas the micrograph that

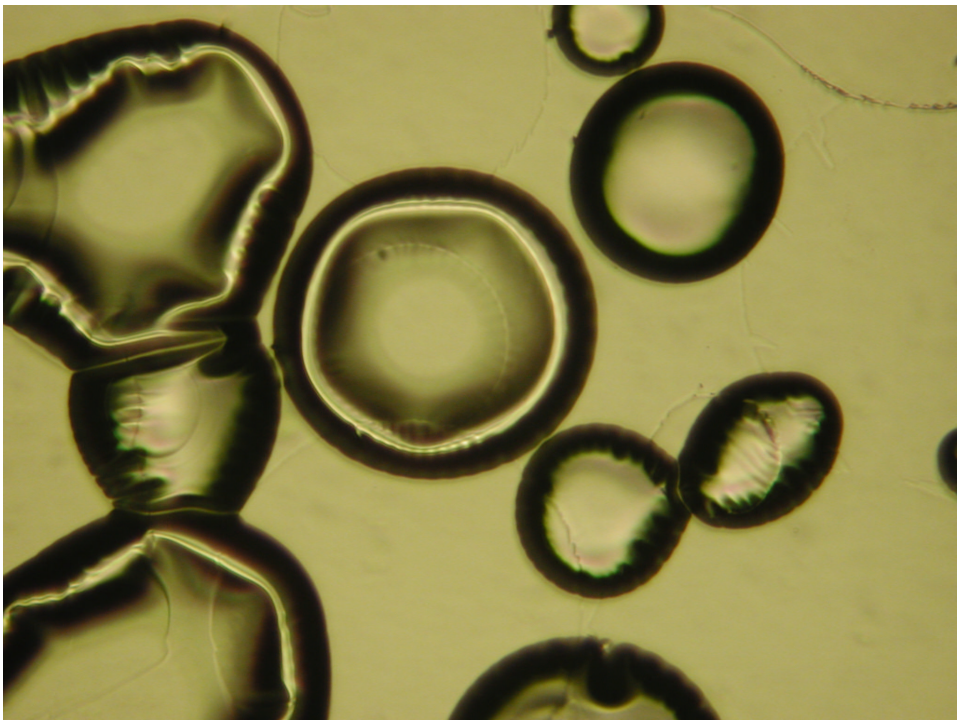


Figure 17: Cratered surface showing a thick shiny layer of amorphous silicon which has delaminated. This sample was the control. The figure is 1 mm across.

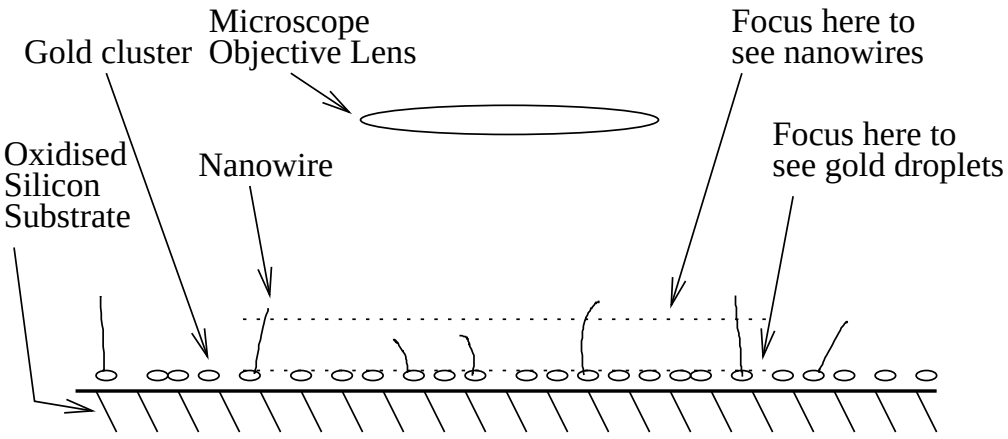


Figure 18: The optical microscope has very limited depth of field. This has the advantage that the height of the nanowires can be seen, but the disadvantage that they may be overlooked.

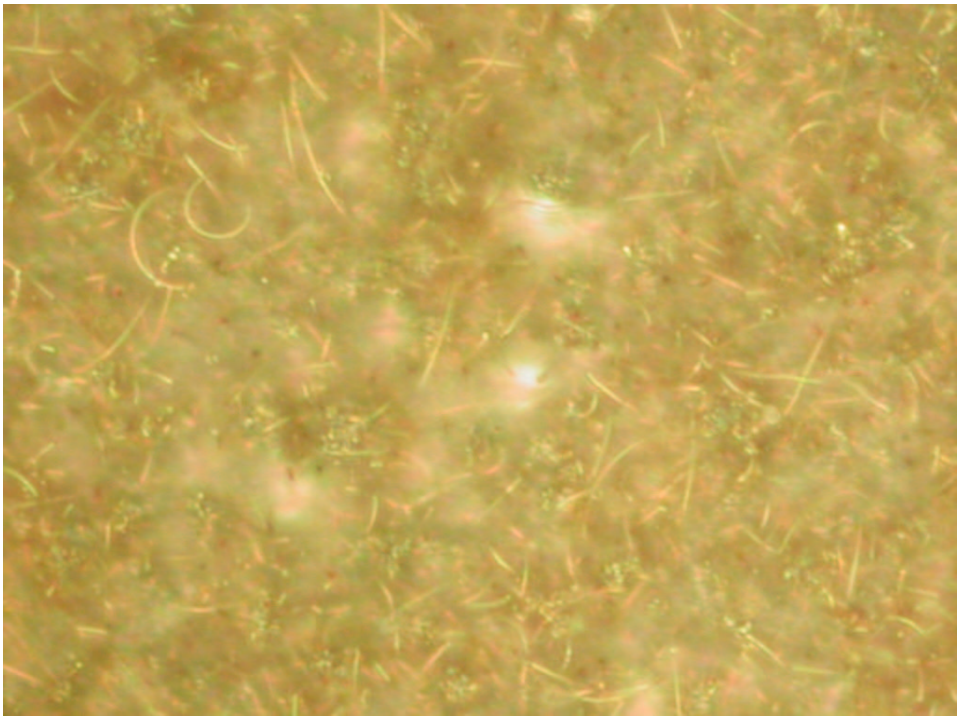


Figure 19: Densely packed silicon nanowires grown on 5 nm of gold. This image from the optical microscope is 100 μm across.

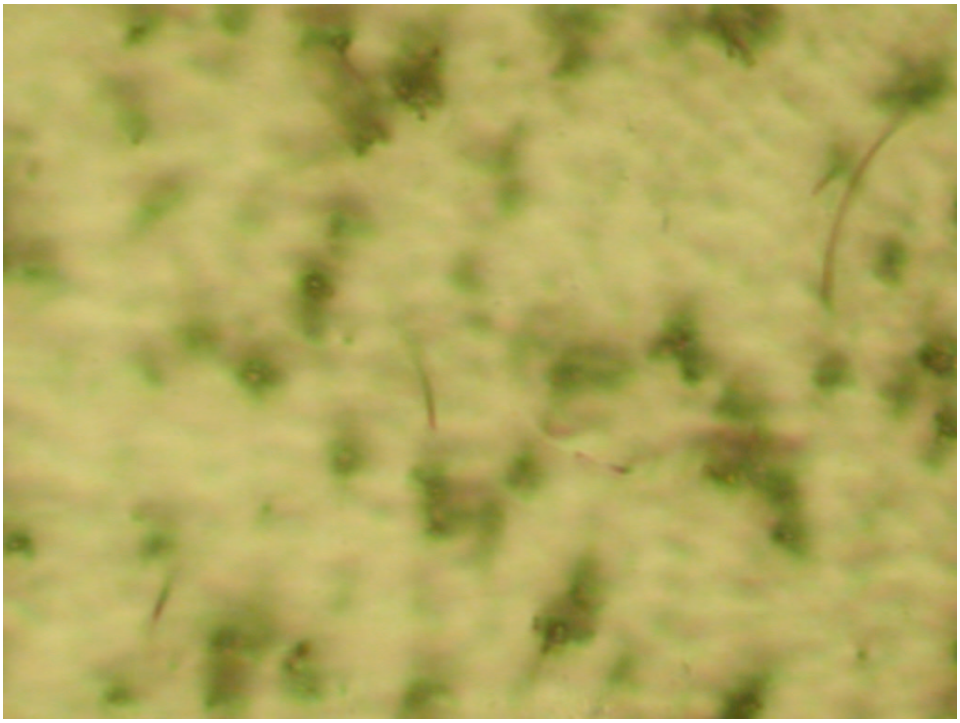


Figure 20: Sparse nanowires can be clearly seen to stand upright. This sample had 5 nm of gold, but on a quartz substrate. This image from the optical microscope is 100 μm across.

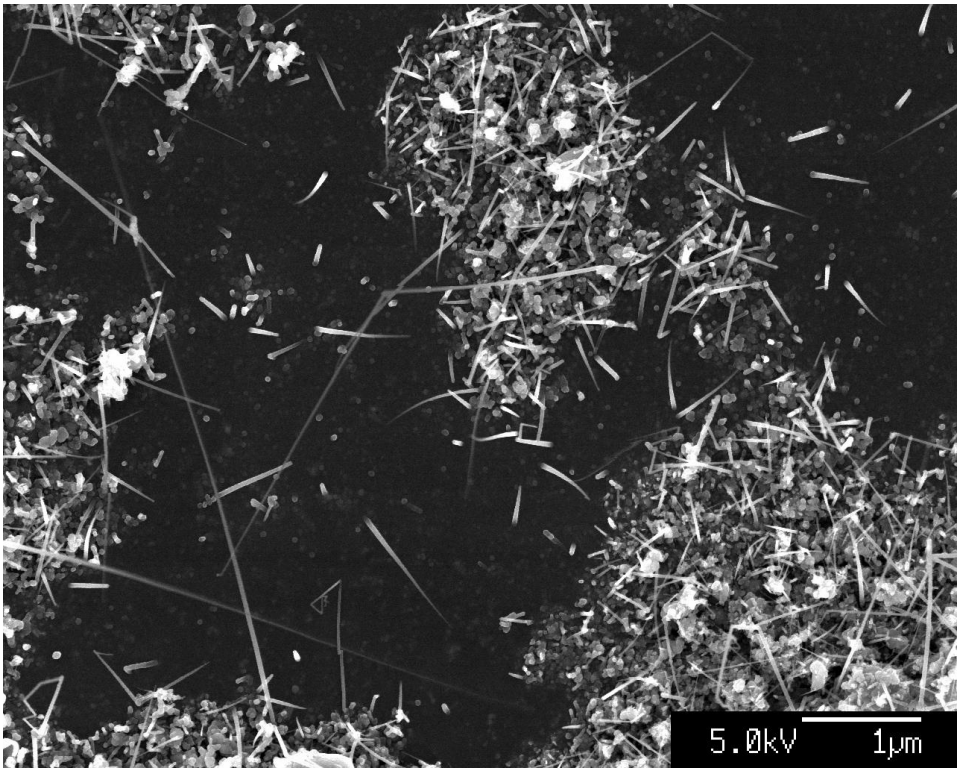


Figure 21: 5 nm Au film, treated with pure silane and showing nanowires in the vicinity of a scratch.

is the most visually informative is the one shown. The microscope has a resolution of approximately 5 nm although this is further limited by vibration and depth of field. Only an upper bound could be established for the width due to the vibration of the wires, the limits of resolution and depth-of-field of the SEM, and the fact that, being very bright, due to secondary electron emission, the wires appear oversize. Alternatively a faint wire only partltopy in focus may appear thinner than it is. Additional difficulties with the SEM arose from charging-up of the substrate[14] and the fact that the electron beam actually distorts and bends the thin wires. It proved most interesting to look at the edges of the gold coating, where it had either been scratched or masked.

- Figure 21 shows nanowires 20 nm wide and up to 5 μm long. These are in an area where the gold film has been scratched: the wires are most dense where the film is intact. The wires taper, although this effect is increased slightly because they stick out from the surface so are not in focus along their entire length.The "blobs" in the background are about 60 nm in size. The conditions were: 5 nm thick gold, 400 ^{o}C at 300 mTorr, 80 sccm silane with 6 W plasma for 15 minutes.

- Figure 22 shows nanowires 50 nm wide and 5 μm long. There are some wires, but there is also a large amount of "grot" in the background: this may be gold which had clustered during the annealing, or it may be amorphous silicon. Figure 23 shows this magnified and at an edge, where one wire can be clearly seen to stand out, although this wire is only 1 μm long. This

[14]Where the substrate was not metallised (eg using the colloidal gold), charge build-up caused difficulty in focusing the SEM and blurred images. This arises because it is impossible to create a barrier thick enough to prevent diffusion, yet also sufficiently thin to allow charge to leak away. A partial work-around us to reduce the electron beam current.

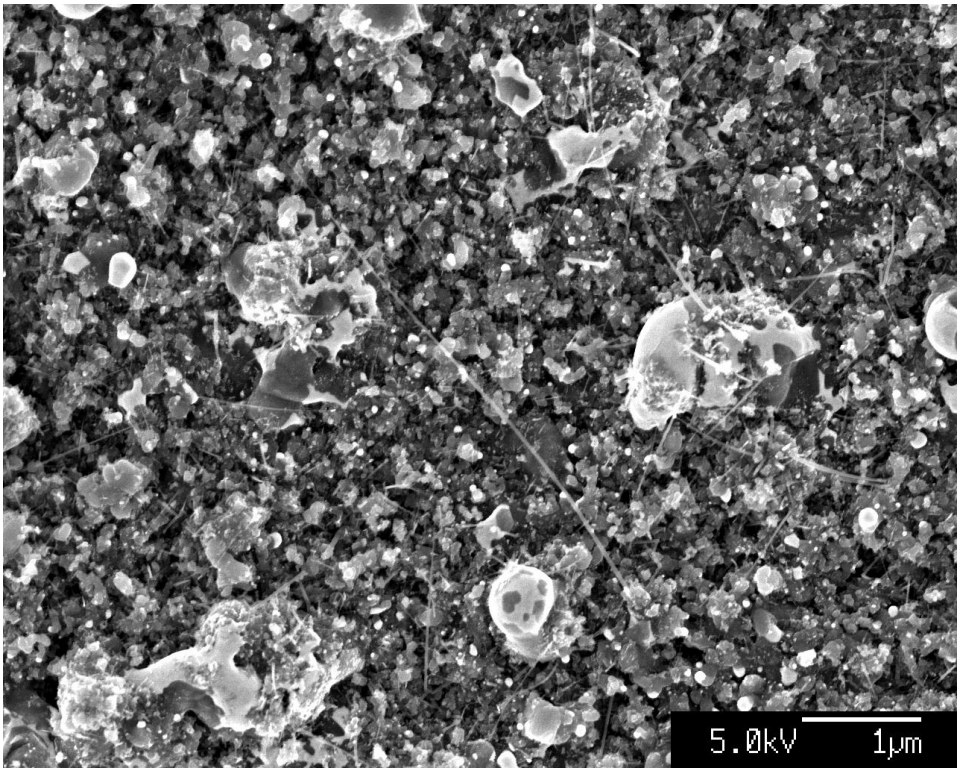


Figure 22: 5 nm Au film pre-heated to 1000 °C in furnace, then treated with pure silane and plasma.

motivates the use of the Au TEM grid. The conditions were: 5 nm thick gold which had been pre-heated to 1000 °C in the furnace, 400 °C at 300 mTorr, 80 sccm silane with 6 W plasma for 15 minutes; the same process conditions as above.

- Figure 24 shows the result of a 5 nm film of iron processed in the DP80 under the same conditions as above. The iron has formed balls between 100-200 nm in diameter, but there are no nanowires at all. The iron was reduced using hydrogen immediately before the silane treatment. This means that oxidation can be ruled out as a potential cause of the failure. Combined with similar results from the optical microscope and the naked eye, it is possible to rule out all of the metals apart from Au at this point.

- Figure 25 shows a few short and fat curved nanowires at most 10 μm long and 500 nm thick. There are also many proto-wires visible, some of which are longer than they appear, since the electron-beam is looking straight down at the surface. The conditions were: 1 nm thick gold, 400 °C at 300 mTorr, 80 sccm silane with 6 W plasma for 30 minutes.

- Figure 26 shows dense, curved nanowires up to 20 μm in length. Figure 27 is closer up, and shows randomly-oriented, curved nanowires. In the background are nodules, probably wires that were unsuccessful. This also shows that the wires protrude from the surface: the free end is vibrating, and is also slightly out of focus due to the depth of field limitations of the microscope. A few very thin wires can also be seen. Figure 28 is a magnified view of a single wire 50 nm in diameter. The wire narrows slightly towards the tip. At the tip, the catalyst nanocluster is clearly visible: it is slightly larger than the wire diameter, as expected. The conditions were as above, except that the gold film was 5 nm thick.

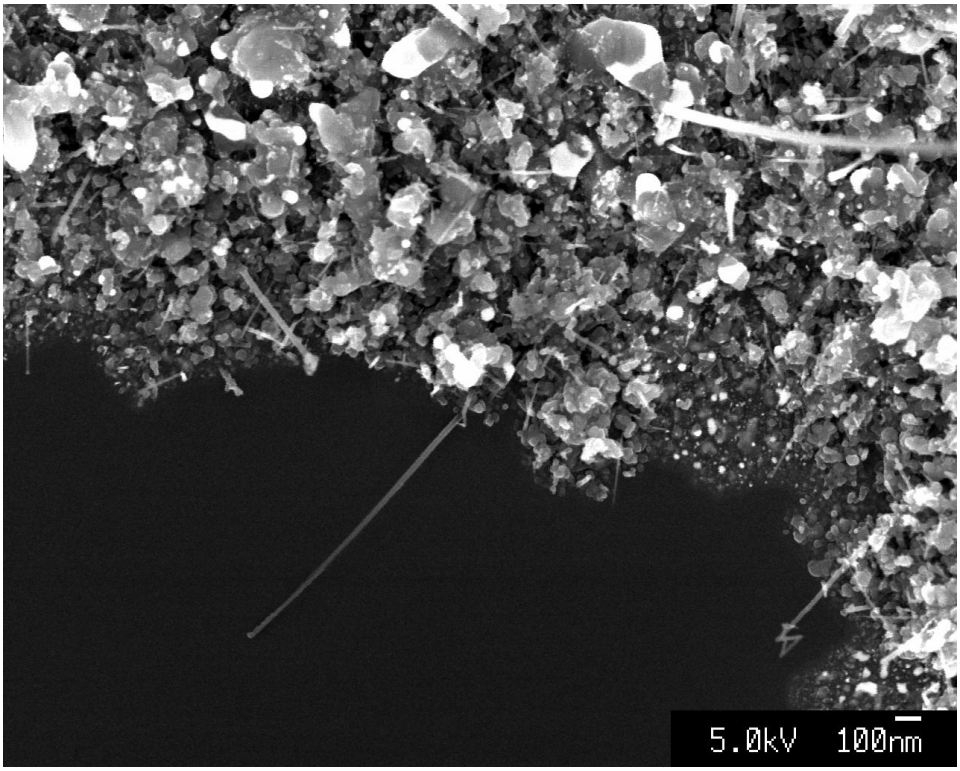


Figure 23: The same as figure 22, but magnified and viewed at an edge.

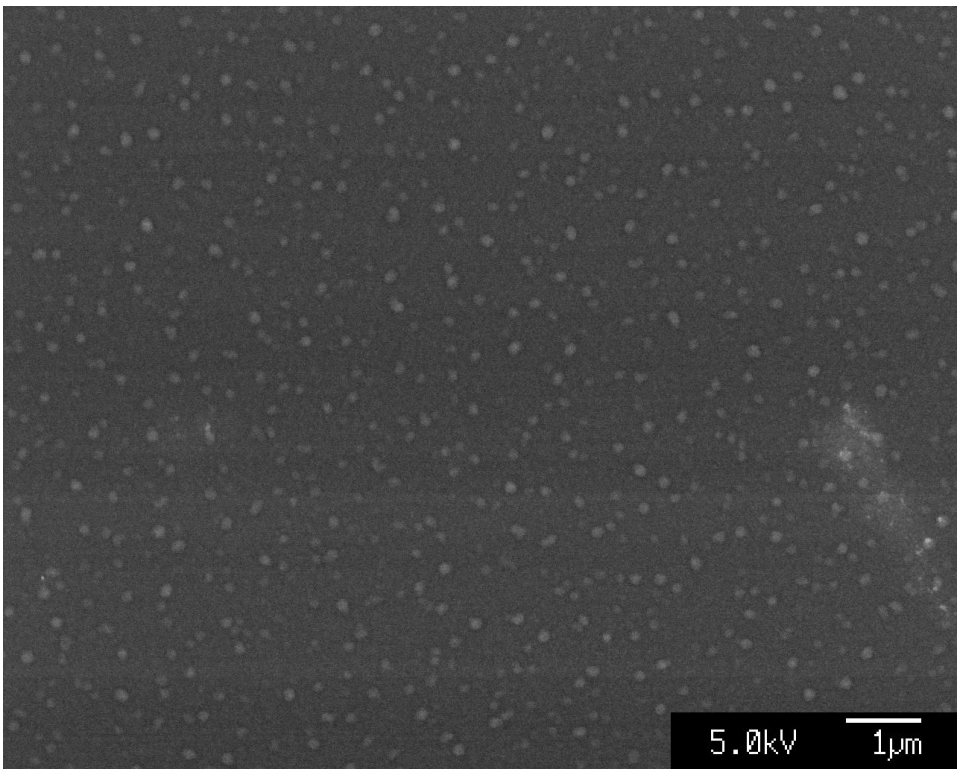


Figure 24: 5 nm Fe film treated with silane and plasma. Although it has formed balls, no wires have grown.

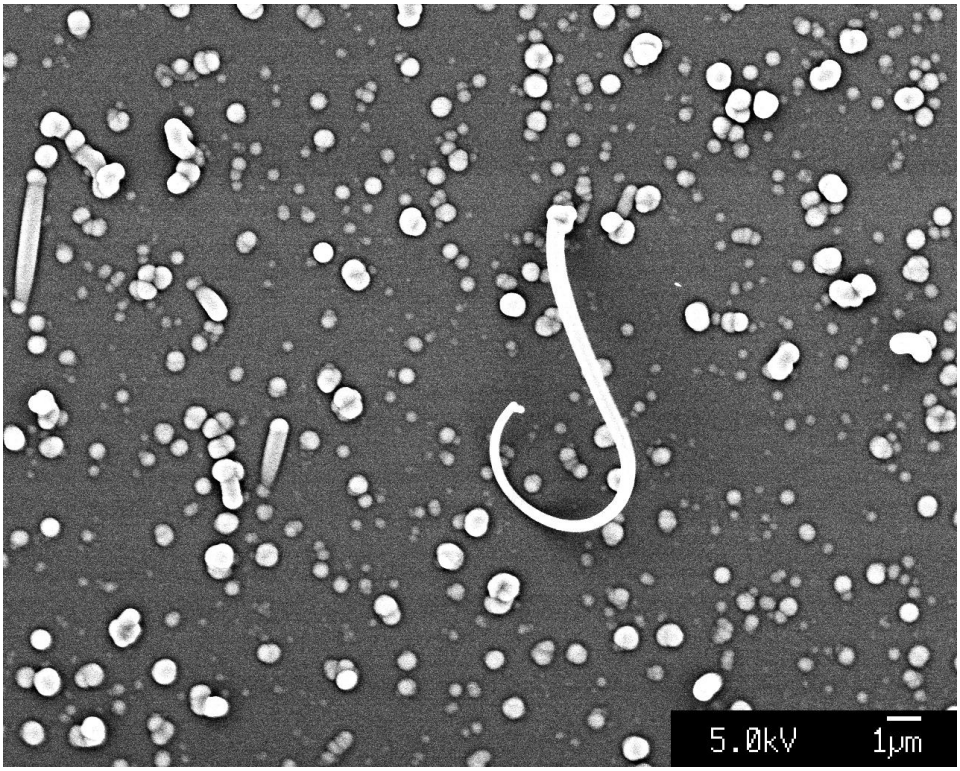


Figure 25: 1 nm Au film, treated with silane and plasma for 30 minutes.

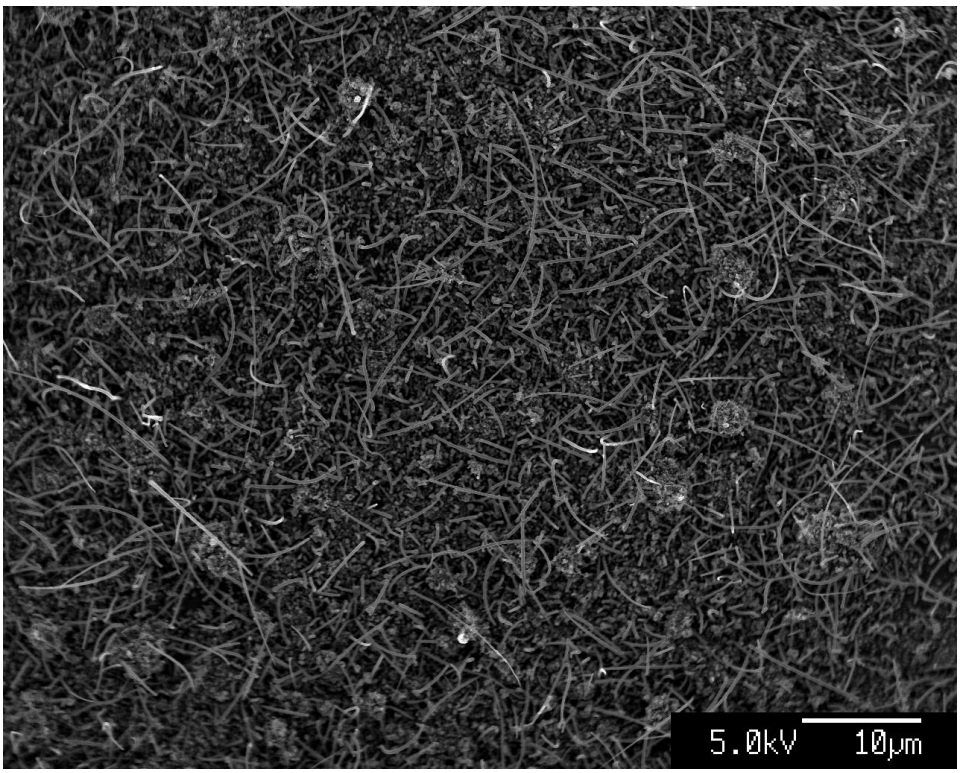


Figure 26: The same as figure 25 except with thicker gold: 5 nm instead of 1 nm.

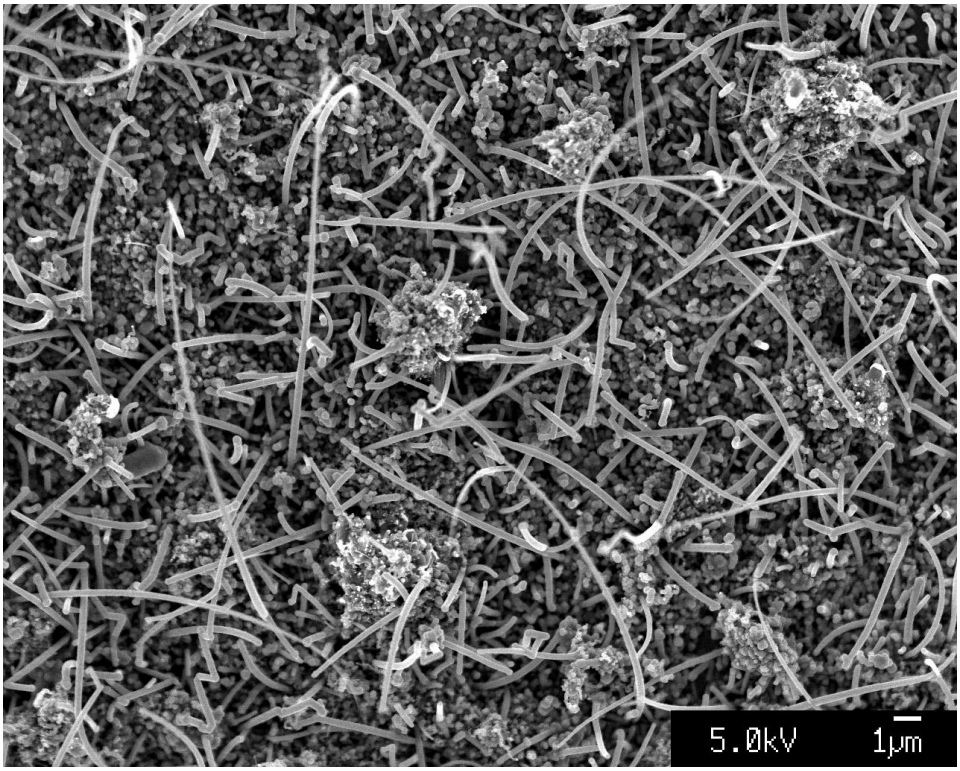


Figure 27: A magnified view of the same thick gold sample as figure 26.

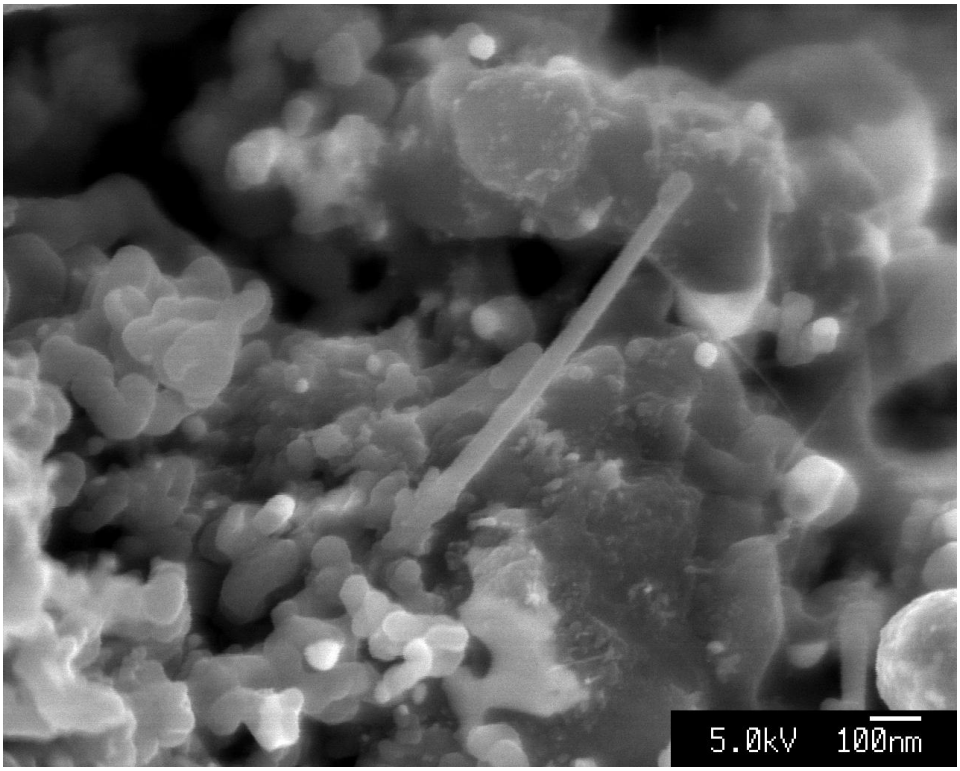


Figure 28: A close up of a single nanowire from figure 27.

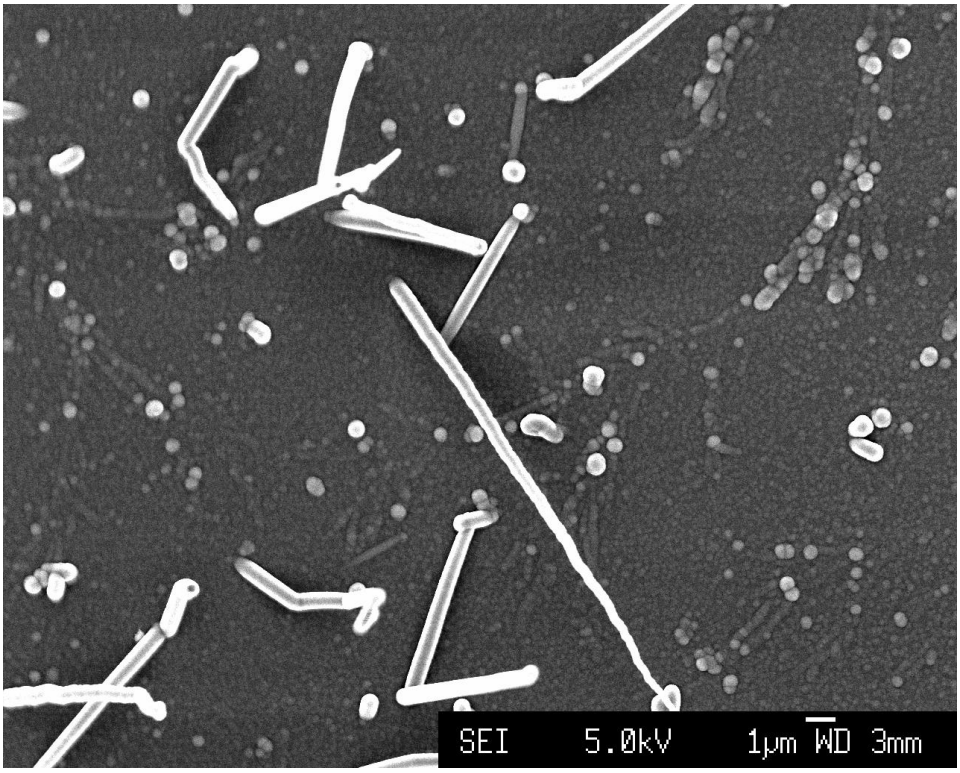


Figure 29: Colloidal gold, treated with silane.

- Figure 29 shows the colloidal gold balls (12 nm diameter) and the resulting nanowires. The balls are the very small objects in the background; where many have agglomerated, there are some short, fat nanowires 500 nm wide and 10 μm long: these get thinner as they grow. Figure 30 shows one such wire: it is straight but contains many sharp kinks - this suggests that it is crystalline, but that the growing surface was unstable. The process conditions were as above.

- Figure 31 shows a gold TEM grid. It is completely covered with nodules, but very few have managed to grow. This may indicate that a great deal of amorphous silicon was deposited, thus covering any wires and preventing them from growing, or it may mean that the hydrogen etched away any wires that began to grow. The DP80 chamber itself was full of polymerised silane, and all the other samples were covered in a thick, shiny sliver layer, suggesting that a great deal of amorphous silicon had been deposited. The conditions were: 400 ^{o}C at 1800 mTorr, 80 sccm silane diluted with 400 sccm hydrogen, 100 W plasma for minutes. This process also suffered from extreme cooling: by the end, the temperature was only 273 ^{o}C.

- Figure 32 shows 200 nm balls of gold which have formed in the DP80 from the initial 5 nm layer. There are also a very few short wires. This sample, with the thick gold film was the best: none of the others worked at all. The conditions were: 400 ^{o}C at 1000 mTorr, 8 sccm silane diluted with 72 sccm helium with 6 W plasma for 30 minutes. This sample should have succeeded: it is possible that the reason for its failure was the very low quantity of silane; itself a consequence of the need to minimise the gas flow so as not to disrupt the temperature excessively.

- Figure 33 shows a 3 nm thick Au film, processed with pure silane and plasma. This is viewed along an edge of where the gold layer was deposited. Where the gold layer is most thick, the

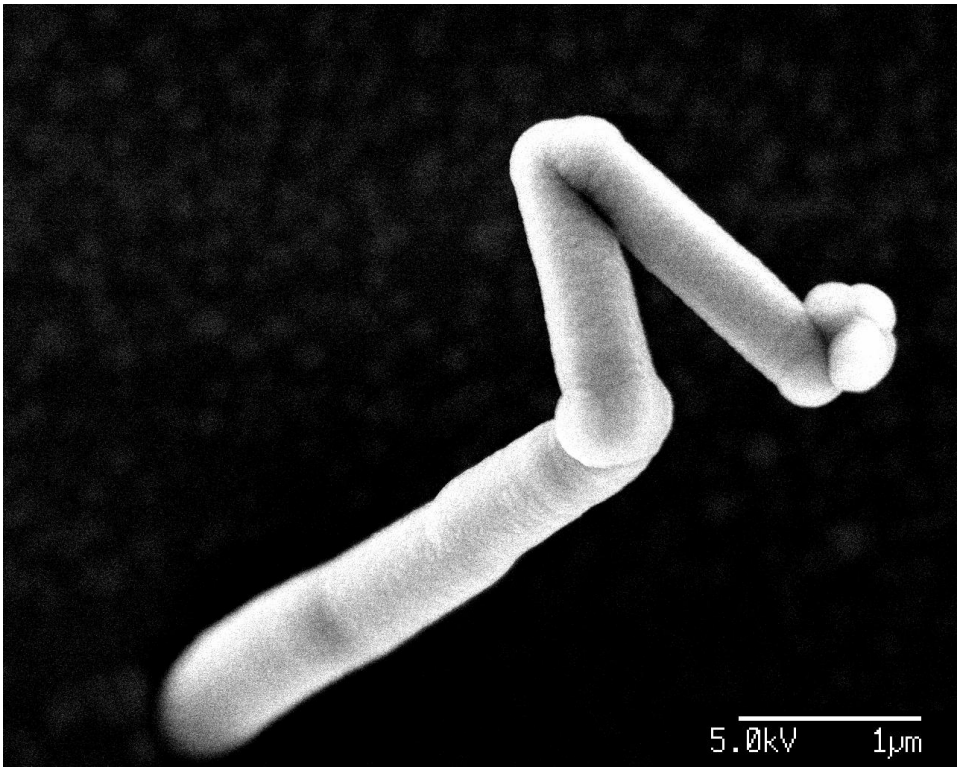


Figure 30: One of the colloidal gold nanowires, showing sharp kinks.

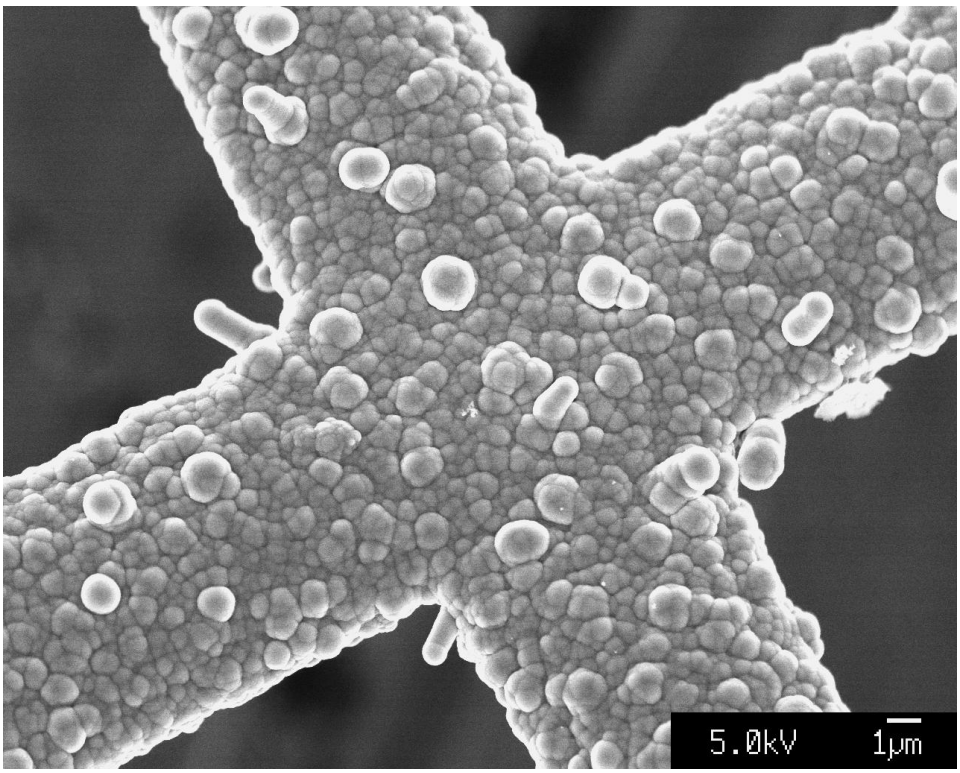


Figure 31: Gold TEM grid treated with Silane diluted 1:5 in hydrogen and 100 W plasma.

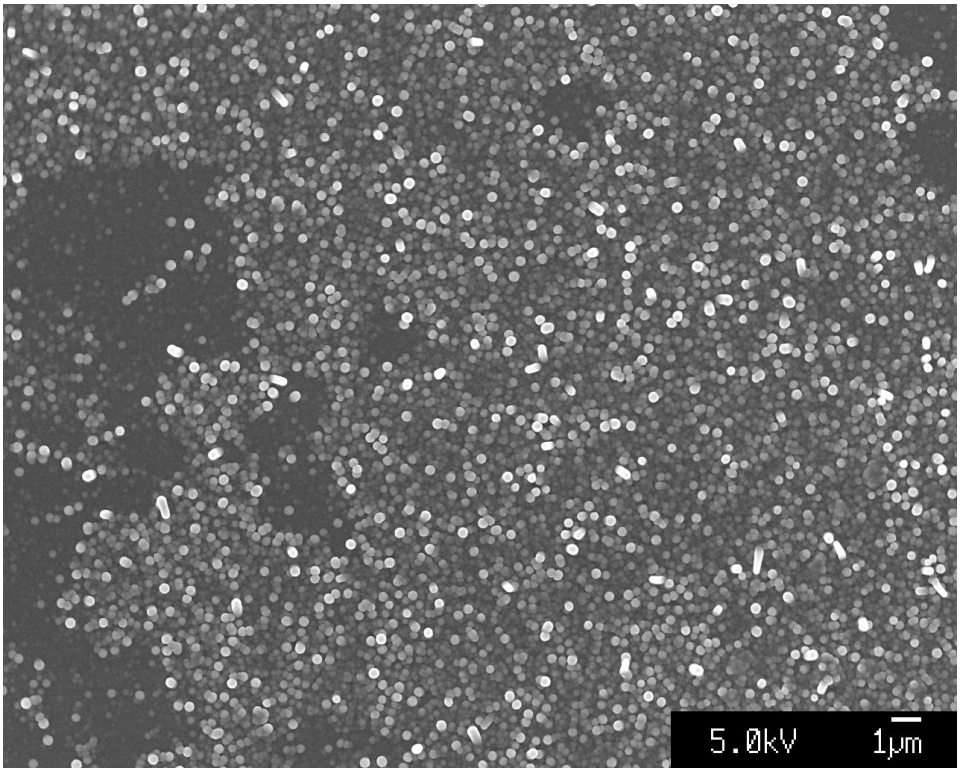


Figure 32: 5 nm gold treated with silane diluted 1:10 in helium, with plasma.

nanowires form a dense, curved forest, however they are less dense where the gold was not initially present. They have moved a few μm either by diffusion of the gold, or, more likely, by being blown there by the ion wind. These wires are as long as 15 μm. Figure 34 shows one long, thin, straight wire 2 μm in length but only 20 nm thick. This indicates that these conditions are promising, and motivates the use of high pressure and pure silane for further optimisation. The conditions were: 400 ^{o}C at 1000 mTorr, 80 sccm of pure silane with 6 W plasma for 30 minutes.

- The attempt to grow thermal nanowires without plasma met with failure. The conditions were 400 ^{o}C at 1000 mTorr, 8 sccm of silane diluted with 72 sccm of hydrogen without plasma for 30 minutes. None of the samples showed any evidence of nanowires in the optical microscope. One sample was examined in the SEM and indeed there were no nanowires. It is shown in section 4.1 as figure 14 as an example of the way that the gold forms small crystals when heated.

- Figure 35 shows some nanowires 20 nm thick and 20 μm long in the empty space within the Au TEM grid. The conditions were: 400 ^{o}C at 1200 mTorr, 80 sccm silane with 6 W plasma for 1 hour.

- Figure 36 shows silicon with 2 nm of Au patterned via a TEM-grid shadow mask. In between the gold areas, there are long filaments of silicon 5-30 μm long and 20-40 nm wide. This demonstrates that the wires can be localised by patterning the gold; that there is an edge effect (the wires grow best at the edges of the Au island, not in the centre); and that it is the Au which is responsible for the wire growth - uncoated areas remain clean. Balls of gold are visible at the start points of the wires. A close-up of one unusual wire is shown in figure 37: this shows

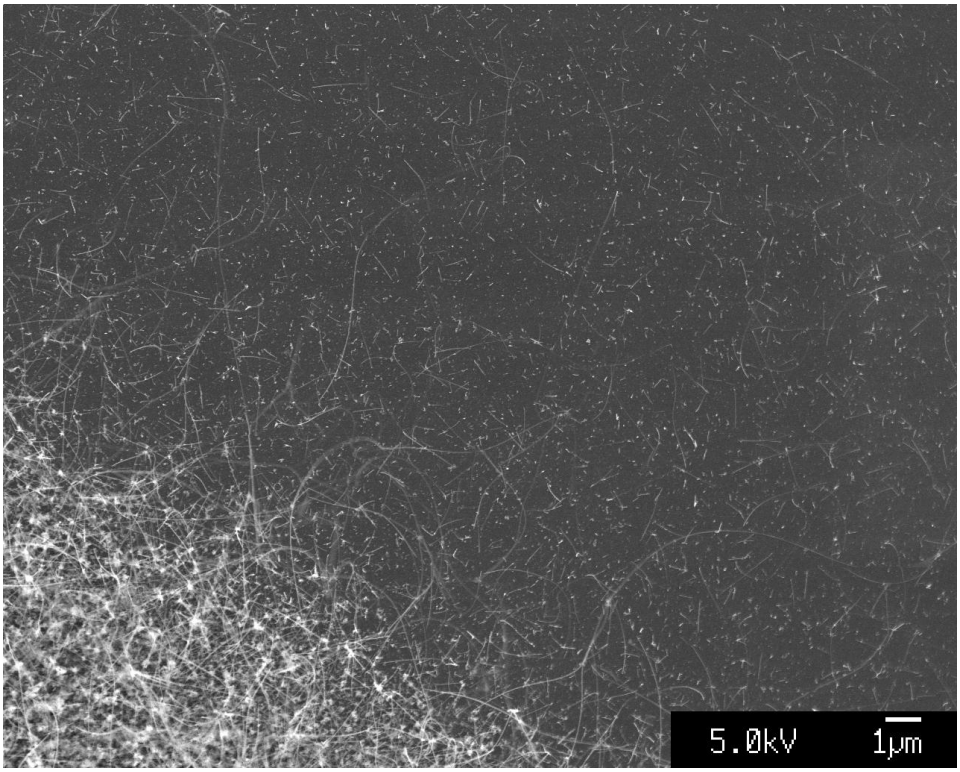


Figure 33: 3 nm gold film processed with pure silane. The edge of the gold film is along the bottom left diagonal where the wires are most dense.

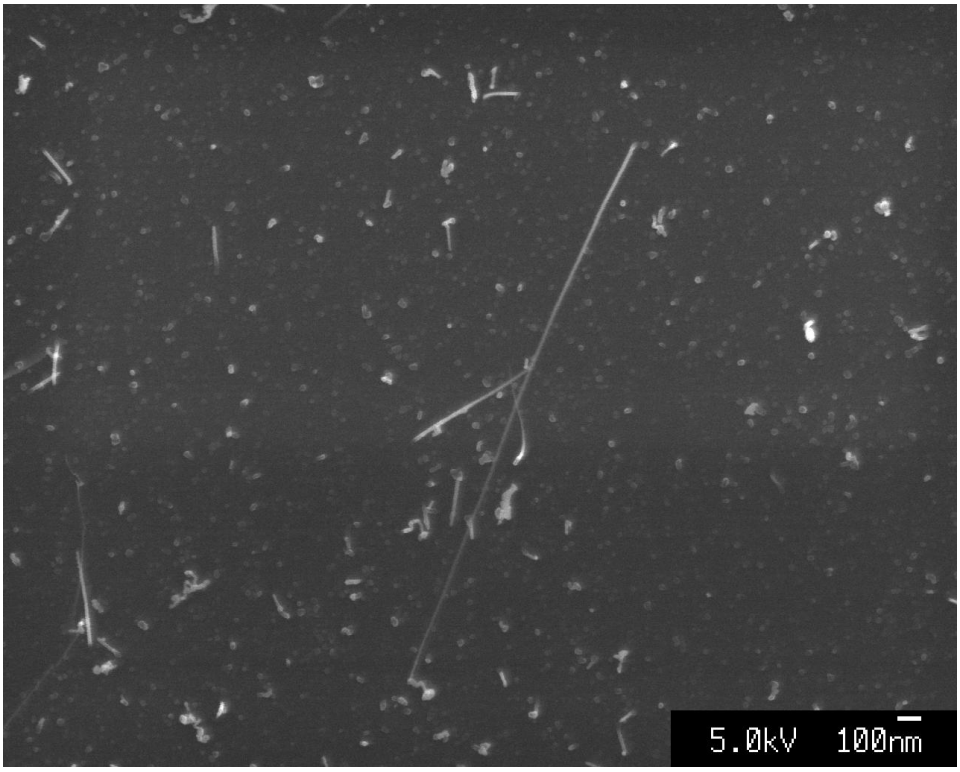


Figure 34: One nanowire from the same 3 nm film as figure 33.

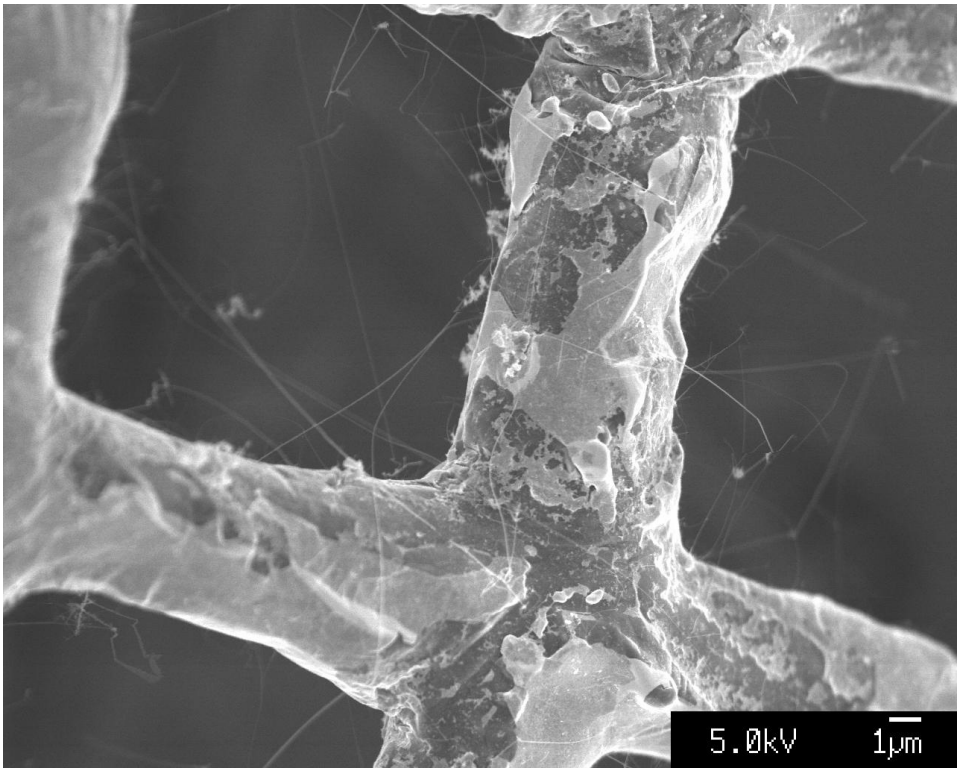


Figure 35: Gold TEM grid treated with silane and plasma.

that the wire is totally straight but also has some sharp kinks. Its straightness demonstrates that it is crystalline. The conditions were the same as above.

- Figure 38 shows a central region within a 2 nm thick 1 mm wide gold dot. Here, in contrast to the edges, there is inadequate space, and the wires coagulate, becoming thick and worm-like. The 3 nm thick gold layer produces very similar thick "worms" 200 nm in diameter. The conditions were the same as above.

- Figure 39 shows the dense forest of nanowires created by a 1 nm layer of gold. These are 20 nm thick and upto 30 μm long. They are shown at closer range in Figure 40, which shows that they are mainly straight and of uniform length.

- Figure 41 shows wires upto 10 μm long and 30 nm thick produced by the colloidal gold. These wires are not very densely packed, although there appear to be many short proto-wires forming a "fluff". Figure 42 shows them at closer range - kinks are also apparent. The process conditions were the same as above.

- Figure 43 shows 5 nm Au at an edge with (left to right), wires that are 120 nm thick and densely packed; the edge of the Au layer with Au droplets visible; and the thinner (40 nm) wires out past the edge. The process conditions for these wires were: 400 ^{o}C at 1000 mTorr, 80 sccm of pure silane with 6 W plasma for 90 minutes

- Figure 44 shows the edge of the 3 nm Au layer with wires grown under the same conditions as above. The Au island has 20 nm thick, 10 μm long wires, after which there is a short gap of

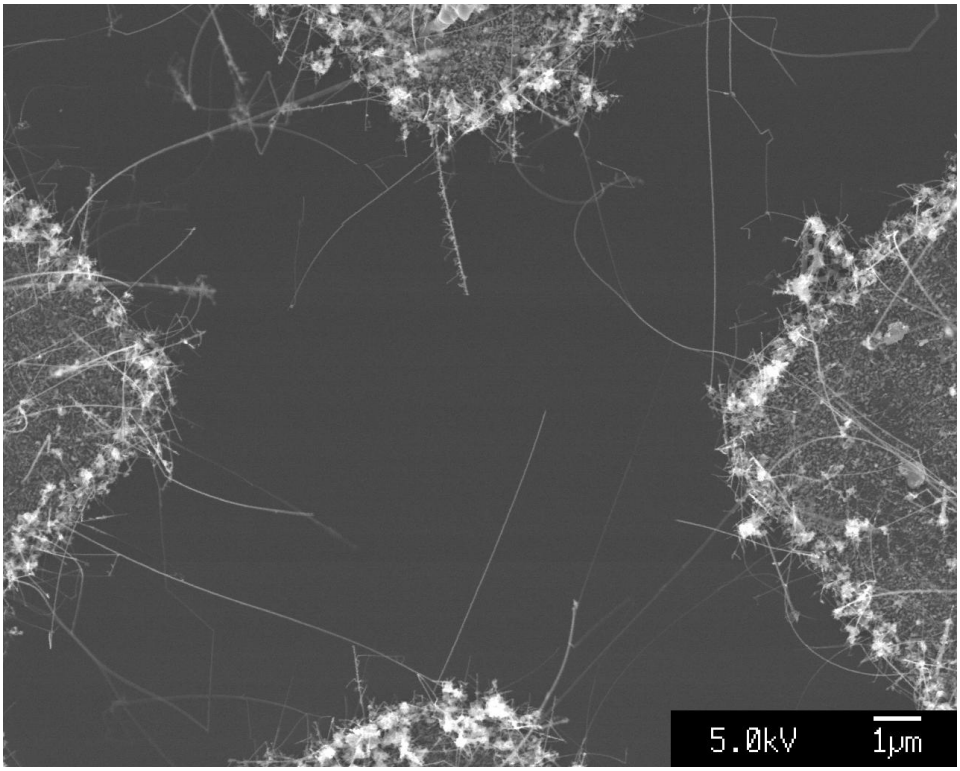


Figure 36: Silicon patterned with 2 nm Au via the Au TEM grid.

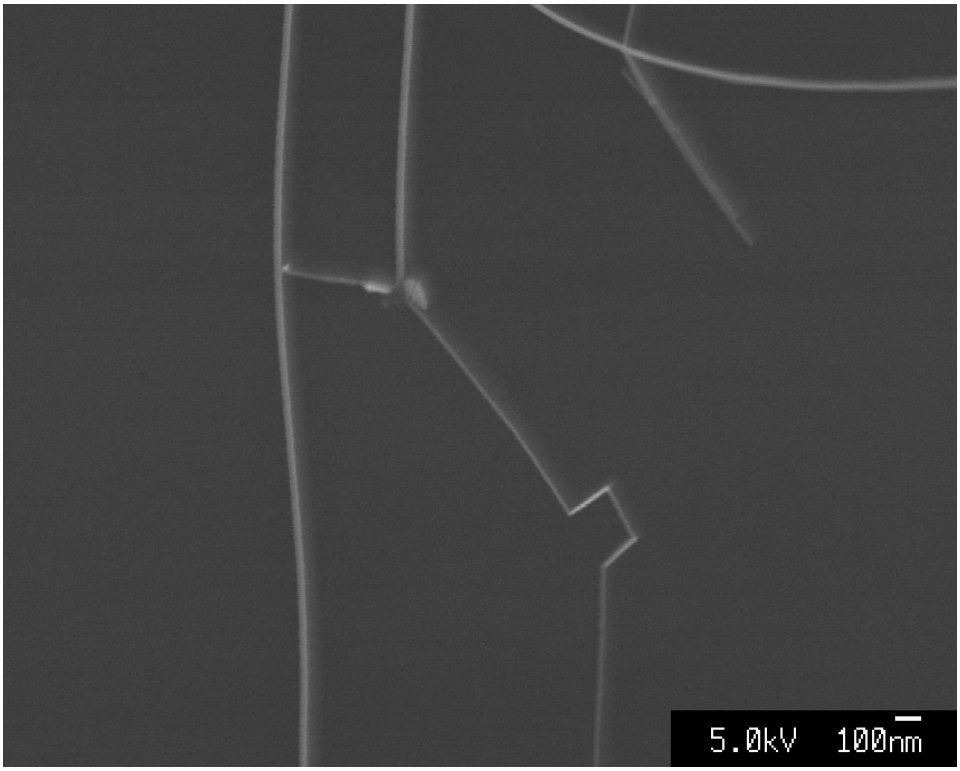


Figure 37: A close-up of one of the wires from figure 36

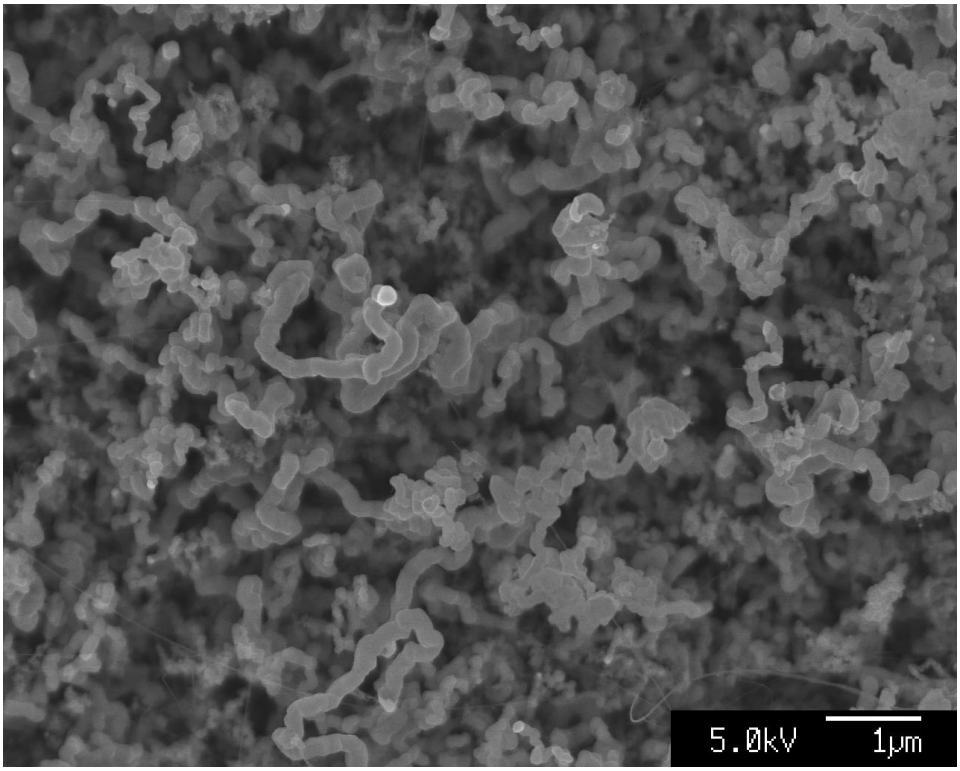


Figure 38: The central region of an area of gold.

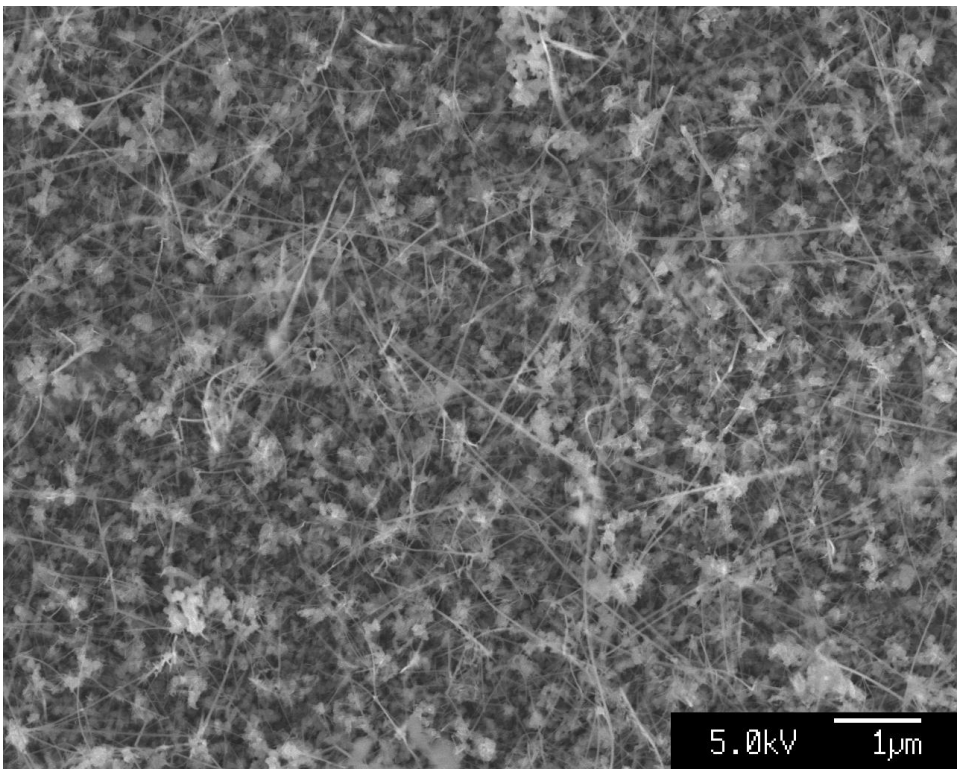


Figure 39: 1 nm gold producing a dense forest of wires.

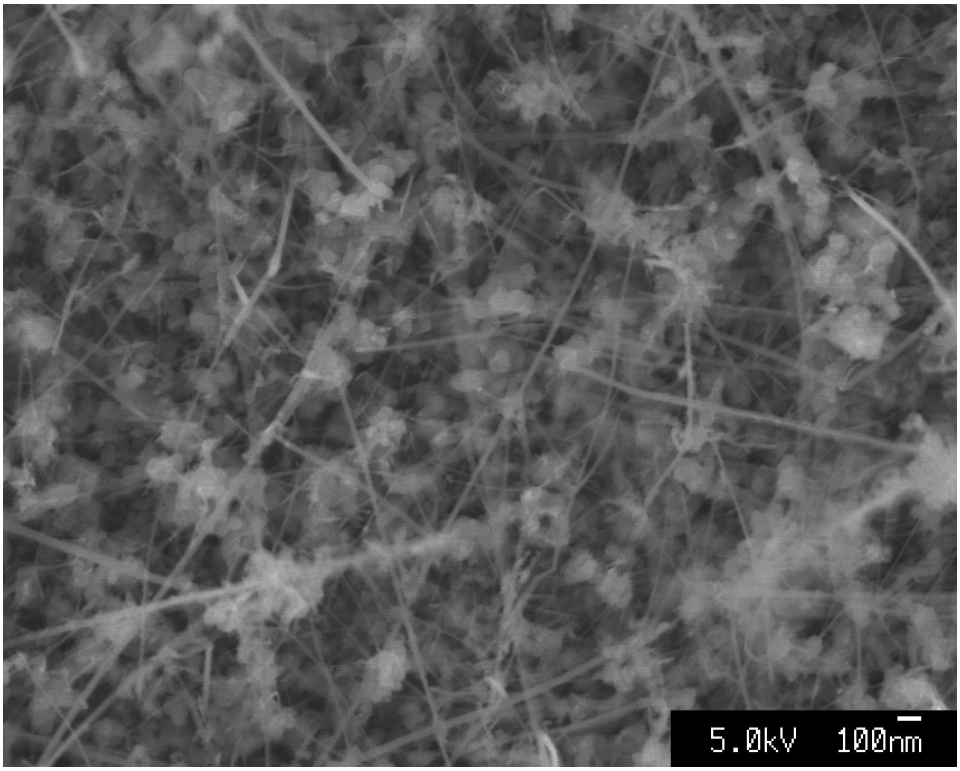


Figure 40: A magnified view of figure 39.

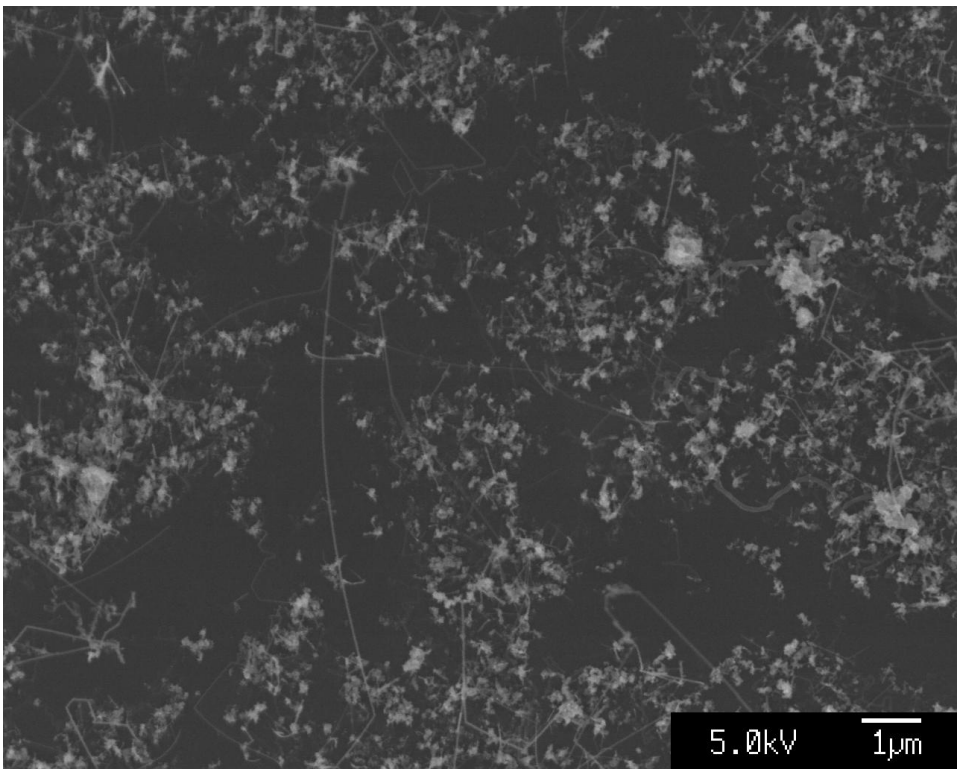


Figure 41: Wires growing from colloidal gold balls.

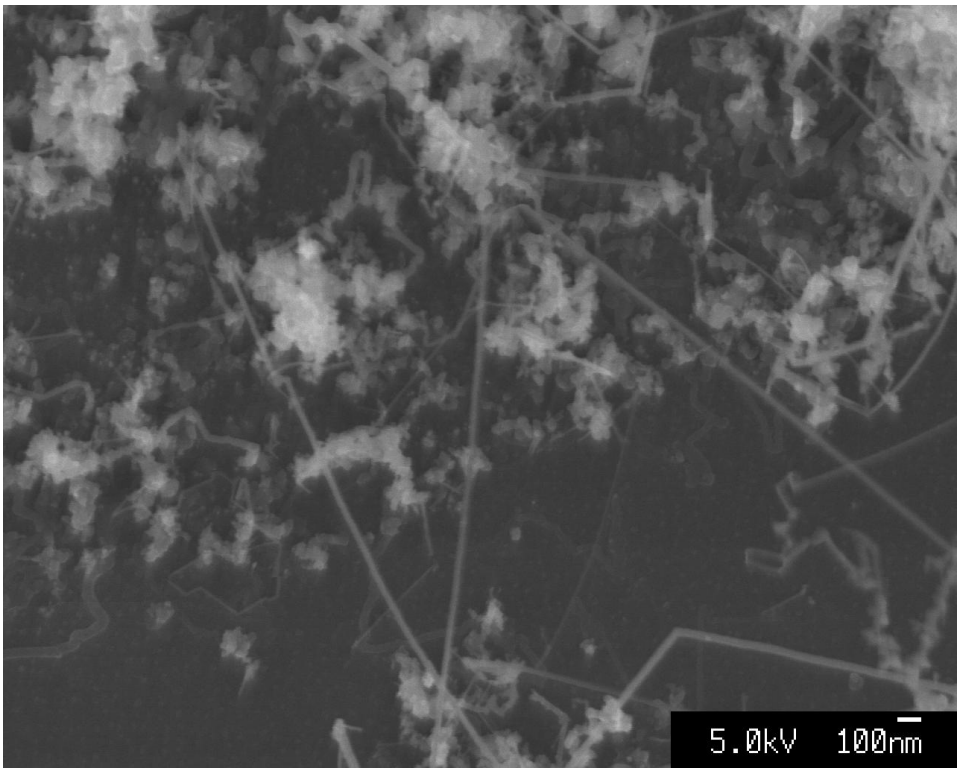


Figure 42: A magnified view of the wires seen in figure 41.

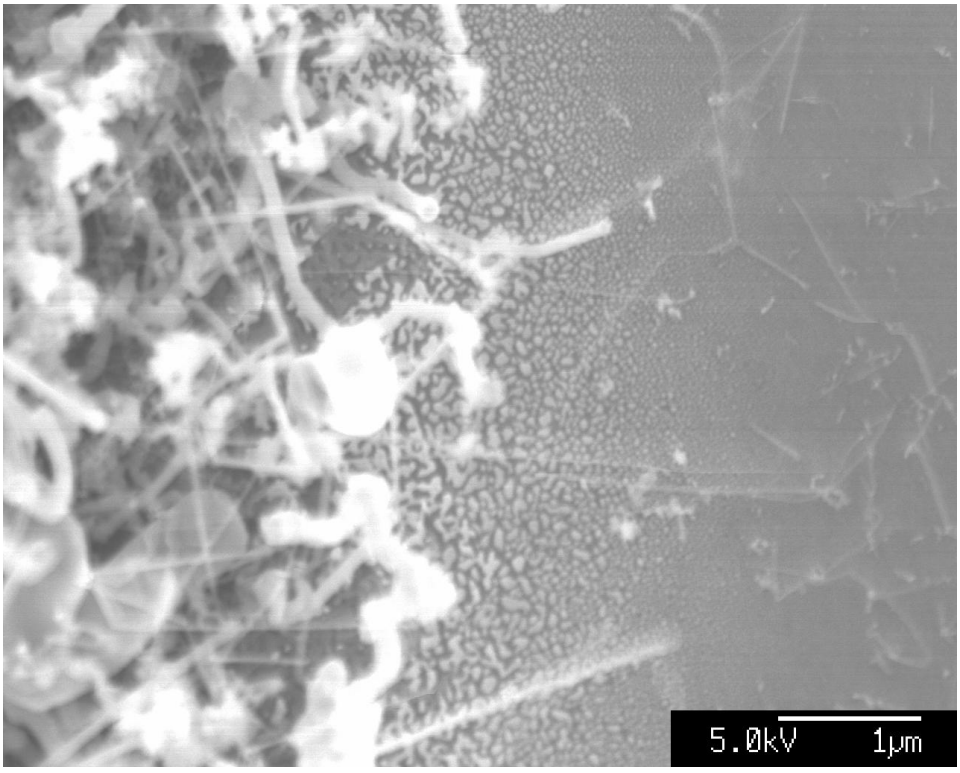


Figure 43: 5 nm Au at the edge. This shows (left to right) : Thick wires where there is Au coating; Au thinning out and visible as droplets; Thin wires out past the edge.

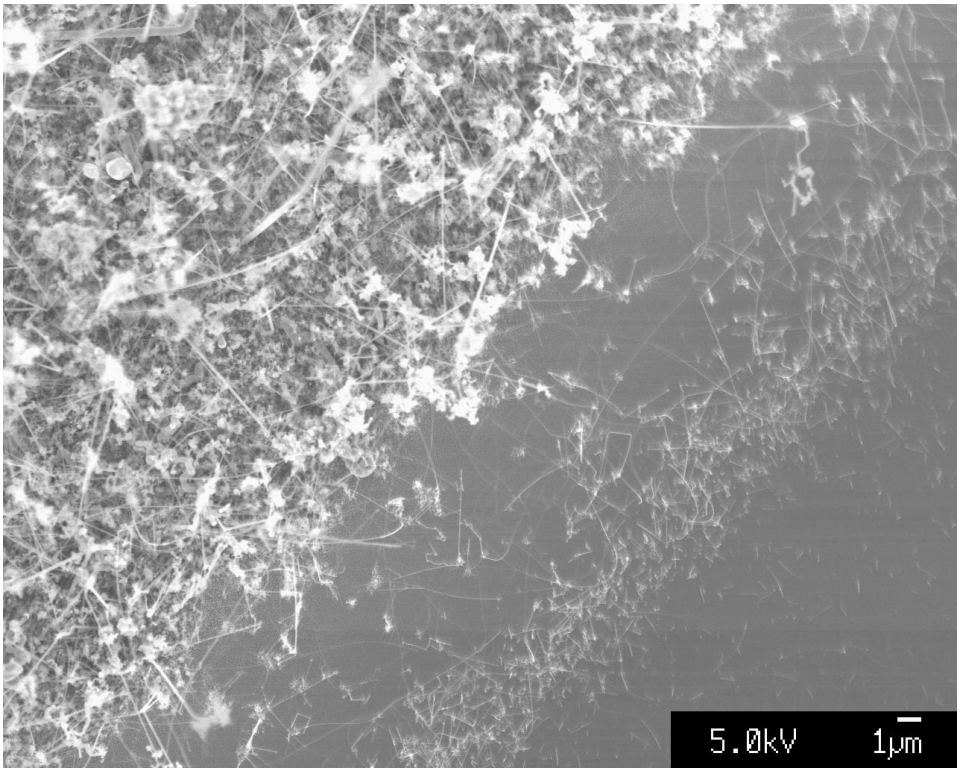


Figure 44: 3 nm Au layer with the Au island in the top left.

8 μm, followed by a 2 μm band of thinner nanowires, followed by uncoated silicon. Figure 45 shows these wires at closer range.

- Figure 46 shows the wires grown using only 1 nm of gold and the same conditions as above. These wires are 20 nm wide and about 7 μm long: they are smaller and more curved than the wires resulting from thicker gold layers.
- Figure 47 shows wires grown from a very thin 0.5 nm layer of gold. These wires are shorter (only 5 μm) and 15 nm thick. Some are also much more curved, although others are straight. Some show kinks. Figure 48 shows one such wire which has nucleated on a 1 μm diameter particle. At the far end, the catalyst ball can be seen, a little wider than the wire. The conditions were the same as above.

Figure 49 shows a very faint outline of patterned 0.5 nm Au. It can be seen that some wires have formed there and are about 0.5 μm long. This demonstrates that the wires may be localised. The growth conditions were the same as above.

4.2.3 Raman Spectroscopy

Some of the samples on quartz substrates were analysed by Raman spectroscopy with the assistance of Dr Andrea Ferrari. This proved inconclusive, showing a mix of amorphous and crystalline silicon. It proved difficult to focus accurately and exclusively on the silicon nanowires (in one case, the 50 kW/m^2 Raman laser sliced a nanowire in half!). Furthermore, the signals were dominated by the

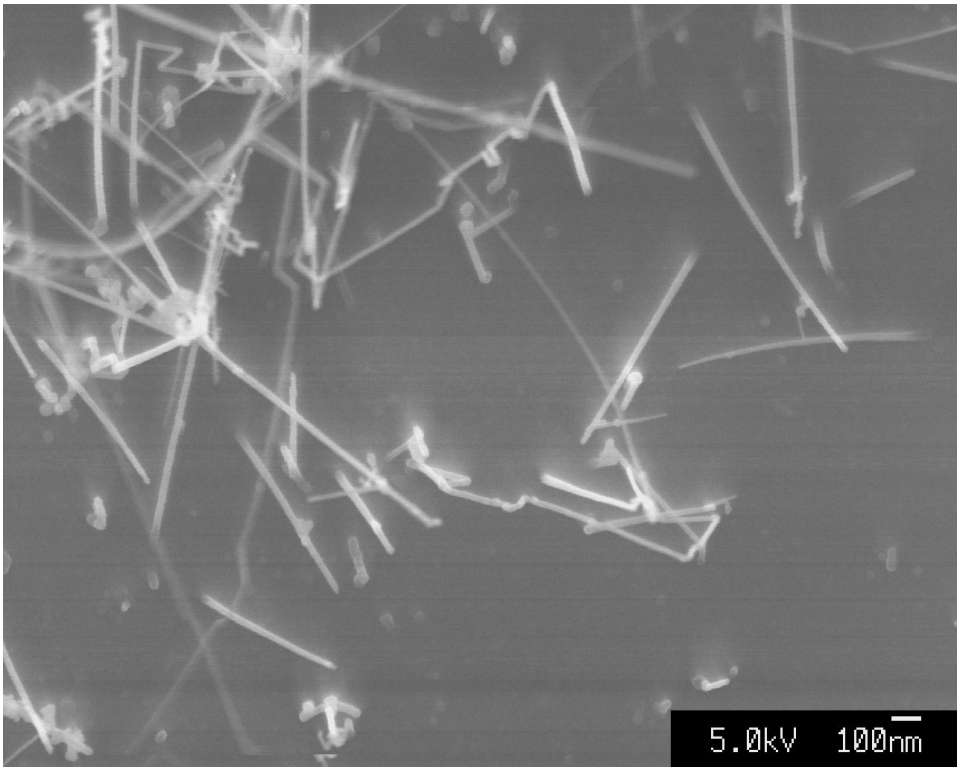


Figure 45: A magnified view of figure 44.

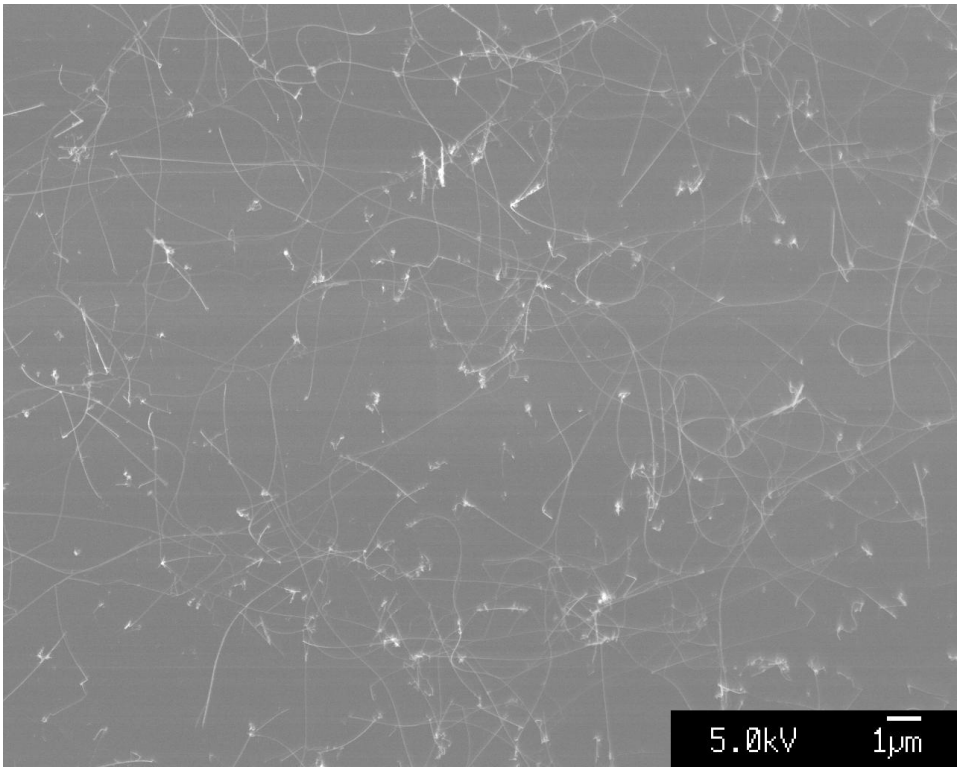


Figure 46: 1 nm Au and its curved nanowires.

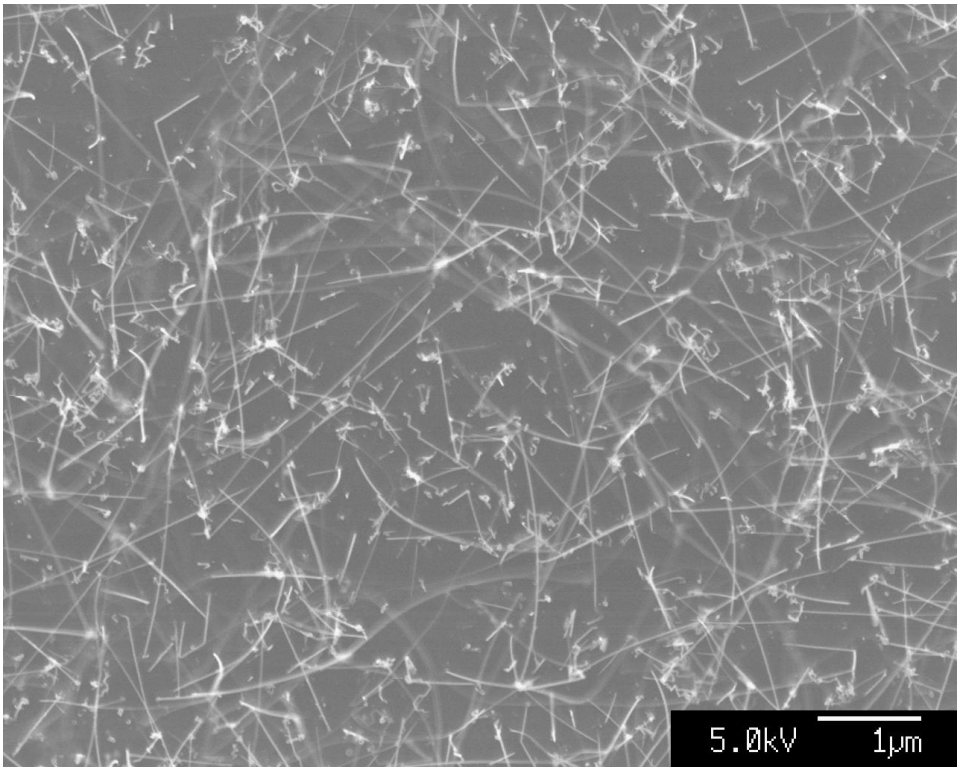


Figure 47: Nanowires grown from 0.5 nm Au.

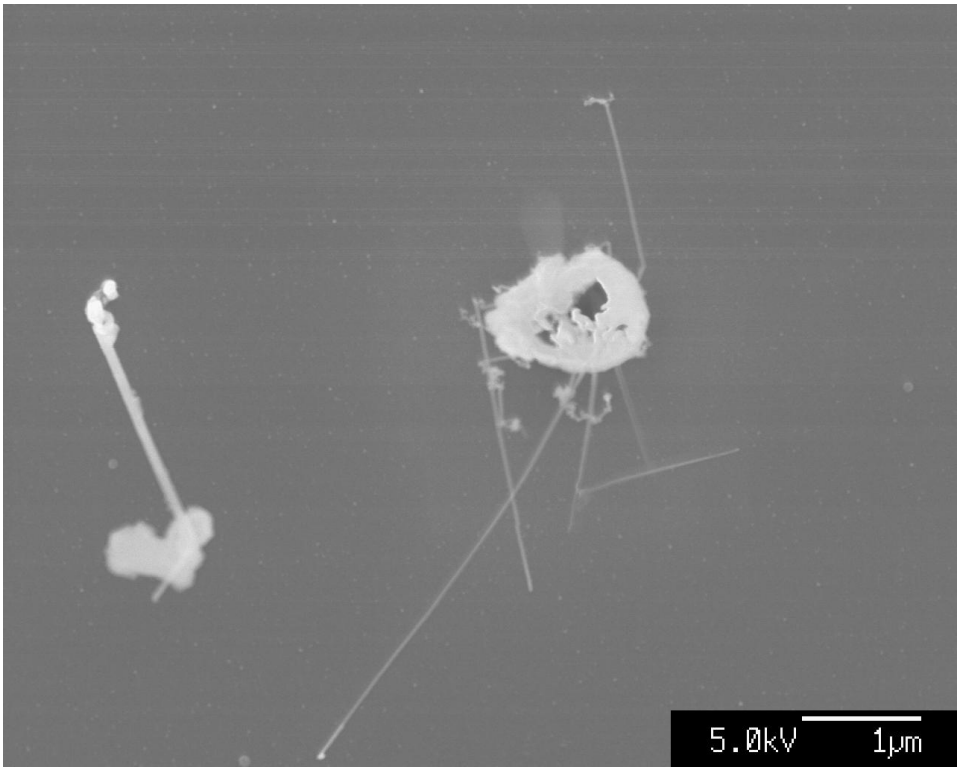


Figure 48: One nanowire at close range.

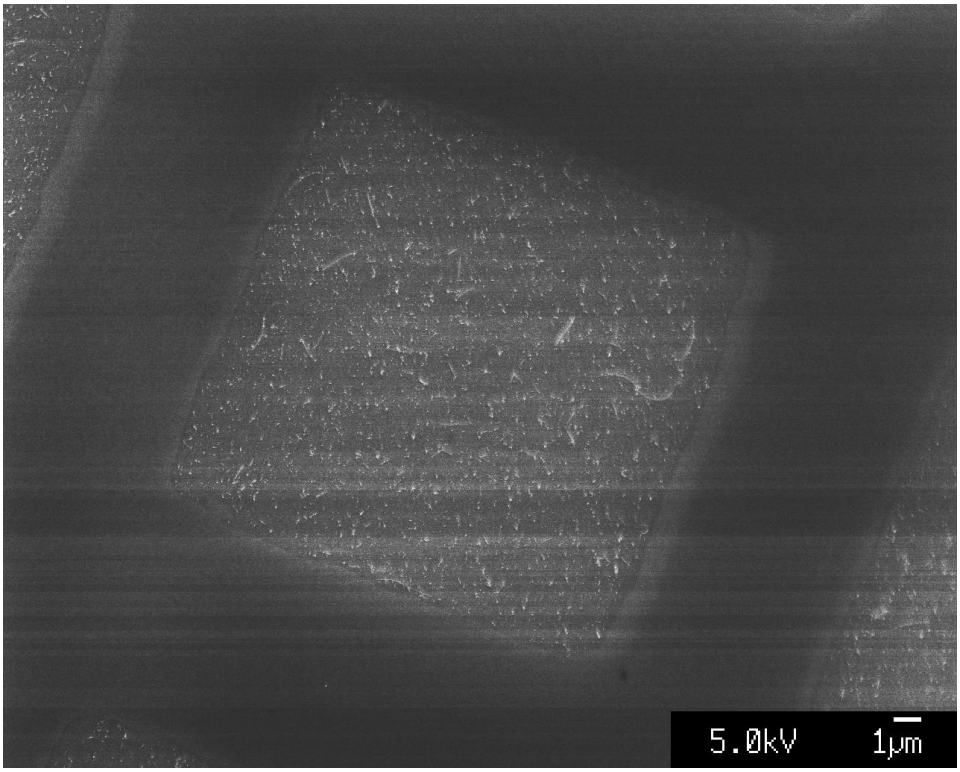


Figure 49: Half nanometer thick gold with nanowires on the island. This image has been strongly enhanced.

response of the gold, which was shown to contain carbon as an impurity. Due to the surface-enhanced Raman-scattering effect, the small signal from the carbon was hugely amplified by the gold metal. It is probable that the wires were crystalline but surrounded by amorphous silicon.

5 Discussion

Silicon nanowires were successfully grown, and the process optimised as far as possible. The wires were upto 30 μm long and as small as 10 nm in diameter. However, this is subject to errors in measurement which may be as large as a factor of 2. The wires were crystalline, and mostly either straight or with sharp kinks where the crystal growth-direction changes. However the thinner wires tended to be curved: this may indicate a partially amorphous nature; or it may mean that the wires have internal stresses arising from lattice distortions. Alternatively, it may be a consequence of distortion by the SEM electron beam.

Of the different catalysts, none worked except for gold. While the phase-diagrams indicate that for fast silicide growth, the Fe/Co/Ni should be liquid, it is theoretically possible to grow the wires without melting the catalyst. However, there was no evidence of success: this means that either the other metals are not usable at all, or that their reactions proceed extremely slowly. Of the metals investigated, gold is by far the best for low temperature VLS. The optical microscope clearly shows that in regions where there is no gold, amorphous silicon is deposited; however, where there is gold, there is nanowire growth combined with the prevention of a-Si deposition.

Changing the catalyst thickness reduced the diameter of the nanowires as expected. There is too much variation between the available samples to measure a precise relationship; this is especially difficult due to the differences in thickness of a factor of 2 between notionally identical thin films from the evaporator.

The use of plasma was proven to be necessary to offset the low temperature. The silane dissociation reaction can occur without plasma, but only at a much lower rate. The initial difficulties with deposition of unknown plaque on the samples (hypothesised to be a-Si) were overcome as the pressure was increased: subsequent samples were largely uncontaminated and contained a high yield of nanowires. Helium dilution was unhelpful: although He assists the plasma to transfer energy to the SiH_4, it reduces the concentration of silane, and slows down the reaction. The use of hydrogen was determined to be counterproductive, although it may benefit from further research to locate the "window" discussed in section 2.4.

The growth of nanowires can occur at temperatures below the critical Au-Si eutectic point at 363 ^{o}C. However reducing the temperature much further slows the reaction rate almost to a stop. As expected, longer reaction times yield longer (but not thicker) nanowires. In agreement with the theory, it was found that higher pressures yield nanowires which are both of higher quality and lower diameter.

Some of the wires are aligned vertically: the tendency to align with the E-field of the plasma is clearly evident, although it is weak and the wires are by no means parallel. If the RF plasma power were increased by a factor of 10, it is expected that the wires would align perpendicularly to the substrate surface; alternatively, this could be achieved by adding a DC bias at the RF power-supply.

The generation of catalyst nanoclusters within the DP80 as it was pre-heated was successful. Utilising a separate process in the furnace proved to be unnecessary, and actually produced less-dense nanowires. However, it is surprising that the 12 nm balls provided by Junfeng Geng were not successful; this is especially striking given that the wires grown from 0.5 nm Au film were of a similar size, and that Westwater et al.[18] report 15 nm wires grown at 320 ^{o}C. The colloidal gold did produce a low yield: these are probably the result of two or more balls agglomerating together to form a larger one. There is a thermodynamic cutoff for the minimum possible size of a nanowire and this is the likely explanation: at low pressure, wires which are too small are unable to grow, due to competition between the surface and volume contributions to ΔG. The experimental evidence suggests that this cutoff occurs somewhere above 12 nm. However, nanowires of approximately 10-15 nm diameter did grow from the thin gold films. This apparent contradiction may be resolved by the oblate nature of the droplets which form from the heated gold film. Since the heated gold produces flattened droplets about 50 times wider than they are high, these are initially between 25 and 250 nm in diameter (resulting from 0.5 and 5 nm gold layers respectively). Thus nucleation and nanowire growth can begin, and only after the droplets have been lifted off the substrate surface by a growing wire do they become more spherical. The success of the 0.5 nm Au film imposes an upper limit on the thermodynamic criterion: thus, experimentally, the critical droplet size for Si nanowire growth is somewhere between 12 and 25 nm in diameter at 360 ^{o}C and 1200 mTorr.

5.1 The Optimal Conditions for Growing Silicon Nanowires

From the experiments performed, the best actual conditions used were: a 0.5 nm thick Au catalyst, 400 °C, 1500 mTorr pressure, 80 sccm flow of undiluted SiH_4 with 6 W of RF plasma. The process was run for 90 minutes. If this work is to be continued in future, it is recommended to begin at 1000 mTorr and an Au film thickness of 5 nm. This guarantees a good starting point. Thereafter, temperatures and pressures should be raised as high as possible[15] The thinner the Au layer, the smaller the resulting nanowires will be. However, there is a point at which wires will no longer grow at all. There is also an element of luck required: around one sample in ten failed randomly. This could have been due to contamination (in one case, out-gassing from the polyimide vacuum tape was implicated), or due to samples being blown over by the gas flow in the DP80.

5.2 Limitations and Problems

The main limitation of this research was caused by the temperature and pressure range of the DP80 plasma deposition system. It is not capable of working at pressures above 2000 mTorr or 400 °C; even these are unattainable in practice. The pressure rating is limited by the gauge and baffle valve, therefore it could be up-rated relatively easily. Similarly it should be possible to up-rate the maximum temperature. However, the most serious problem is that, at a given set-point, the DP80 cools as the gas flows through it, and, although set to 400 °C, it cannot maintain temperatures above 320 °C at even moderate gas flows. This is shown in figure 50 which shows data from the experiments performed. This can be fixed by up-rating the maximum heater *power*; the maximum *temperature* need not be changed.

The project rationale, and the choice of the DP80 system was based upon the gallium low-temperature VLS method. When this has to be abandoned to prevent the contamination of shared facilities, the Au-Si reaction was chosen as a substitute. However this normally requires high pressure and moderate temperature (> 500 °C) to allow thermal growth of nanowires. This was compensated by the use of plasma to aid silane dissociation; however this results in some contamination by amorphous silicon. To correct for that, dilution with H_2 was proposed but it was not successful.

The lack of hydrogen was not a serious impediment in that its use had already been ruled out by the limited experimental data already attained. Nevertheless, further investigation might have been of interest. Given the opportunity, further analysis with an electron microscope, especially one of higher resolution, would have been useful, and would have permitted more accurate measurements of the nanowire diameters.

As with any research, the work performed for this thesis suffered from its share of setbacks. The process of oxidation, gold-coating, and silane deposition requires the concurrent functionality of all three items of equipment: the furnace, the evaporator, and the DP80. Difficulties included failure of the quartz furnace tube on two occasions with subsequent delays for repair; two instances of accidental destruction of the evaporator's glass bell jar; the exhaustion of the high purity hydrogen; and damage

[15] Note that 400 °C is already outside the practical DP80 thermal envelope, and 1500 mTorr is outside the approved pressure range. Therefore a different equipment rig will be needed.

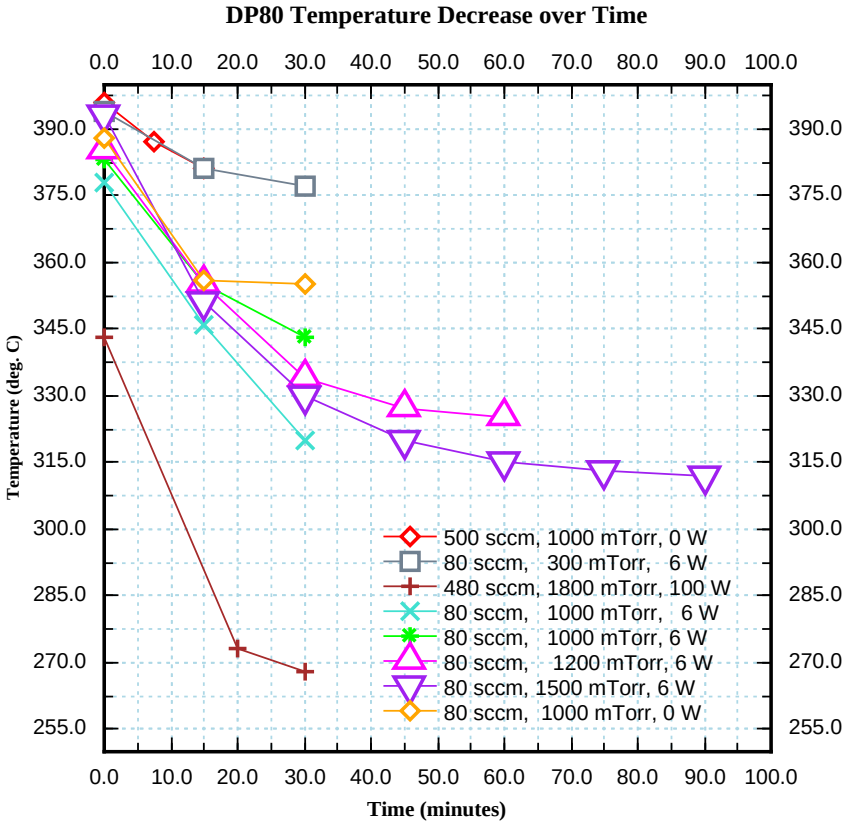


Figure 50: The DP80 is cooled by the gas flow through it.

to the gas scrubber on the part of the author. These all caused delays but, with the exception of the hydrogen (which is, 3 months on, still awaiting shipment by BOC from the Far East) were fixed as quickly as possible by members of the group.

6 Conclusions

This research aimed to investigate the low temperature methods for growing silicon nanowires. This was successful. Starting from a wide range of possible conditions, various permutations were tested, and the process parameters were optimised. This starting point can be built upon to measure more precisely the relations between process conditions and nanowire growth, or it may be used as a reliable method of production of silicon nanowires whose applications may then be investigated. This work builds upon that of others to extend further the lower limits of pressure and temperature for gold-catalysed VLS growth: some more of the lower part of figure 11 may now be filled-in and reported as successful.

6.1 Proposals for Future Research

This research investigated methods for the growth of silicon nanowires at low temperature and low pressure. With the aid of plasma, it was found that nanowires can be grown, however they are not of particularly high quality. Thus future work could continue from the optimal conditions given above, and work at higher pressure in different equipment. Thermal nanowires are also of better quality; therefore higher temperatures of at least 700 ^{o}C should be used in order to enable growth without plasma. It is suggested that either the Silane/STM rig should be used, or that the DP80 should be modified to allow both higher pressures and higher heater power. The use of zinc as an intermediate temperature catalyst[19] has not been much studied: this could prove fruitful. Once nanowires can be grown predictably, they can then be tested in some of the promising potential applications listed in section 1.1.

References

[1] "*Si Nanowires Grown via the Vapour-Liquid-Solid Reaction*"
J. Westwater, D.P. Gosain and S. Usui, Phys Stat Sol (a) 165, 37 (1998) pp 37-42

[2] "*Chemistry and Physics in One Dimension: Synthesis and Properties of Nanowires and Nanotubes*"
J. Hu, T. Odom and C.M. Lieber, Acc. Chem. Res. 1999, 32, pp 435-445

[3] "*Gaining Light from Silicon*"
L. Canham, Nature, Vol 408, 23 November 2000 pp 411-412

[4] "*Optical Gain in silicon nanocrystals*"
L. Pavesi, L. Negro, C. Mazzoleni, G. Franzio and F. Priolo, Nature, Vol 408, 23 November 2000 pp 440-444

[5] "*Surface Chemistry of Silicon Nanoclusters*"
A. Puzder, A.J. Williamson, J.C. Grossman and G. Galli, Physical Review Letters Volume 88, Number 9, 4/03/2002

[6] "*Control of the Size and Position of Silicon Nanowires Grown via the Vapor-Liquid-Solid Technique*"
J. Westwater, D. Gosain and S. Usui, Jpn. J. Appl. Phys. Vol 36 (1997) pp 6204-6209

[7] "*Logic Gates and Computation from Assembled Nanowire Building Blocks*"
Y. Huang, X. Duan, Y. Cui, L. Lauhon, K. Kim and C.M. Lieber, Science, Vol 294, 9 November 2001 pp 1313-1317

[8] "*The Incredible Shrinking Circuit*"
C.M. Lieber, Scientific American, September 2001, pp 59-64

[9] "*Controlled growth and electrical properties of heterojunctions of carbon nanotubes and silicon nanowires*"
J. Hu, M. Ouyang, P. Yang and C.M. Lieber, Nature, Vol 399, 6 May 1999 pp 48-51

[10] "*Controlled Li doping of Si nanowires by electrochemical insertion method*"
G.W.Zhou, H. Li, H.P. Sun, D.P. Yu, Y.Q. Wang, X.J. Huang, L.Q. Chen and Z. Zhang, Applied Physics Letters Vol. 75 (1999) pp 2447-2449

[11] "*Nanotubes and Nanowires for Molecular level Imaging and Detection*"
C. M. Lieber, BioMEMS and Biomedical Nanotechnology, September 2001.

[12] "*Diameter controlled synthesis of single-crystal silicon nanowires*"
Y. Cui, L.J. Lauhon, M.S. Gudiksen, J. Wang, C.M. Lieber, Applied Physics Letters 78,15 (2001) pp 2214-2216

[13] "*A Laser Ablation Method for the Synthesis of Crystalline Semiconductor Nanowires*"
A.M. Morales and C.M. Lieber, Science Vol 279, 9th January 1998 pp 208-211

[14] "*Bulk synthesis of silicon nanowires using a low-temperature vapor-liquid-solid method*"
M. Sunkura, S. Sharma and R. Miranda, Applied Physics Letters Vol 79, (10) 3 September 2001 pp 1546-1548

[15] "The Science of Crystallization: Microscopic Interfacial Phenomena"
W.A. Tiller, Cambridge University Press, 1991, pp 346

[16] "*Morphology and growth mechanism study of self-assembled silicon nanowires synthesized by thermal evaporation*"
Z. Zhang, X. Fan, L. Xu, C. Lee and S. Lee, Chemical Physics Letters 337 (2001) pp 18-24

[17] "*Germanium Nanowire Growth via Simple Vapor Transport*"
Y. Wu and P. Yang, Chem. Mater. 2000, 12, pp 605-607

[18] "*Growth of silicon nanowires via gold/silane vapour-liquid-solid reaction*"
J. Westwater, D.P. Gosain, S. Tomiya, S. Usui and H. Ruda, J. Vac. Sci. Technol. B 15(3) May/Jun 1997 pp 554-557

[19] "*Silicon Nanowires: Preparation, Device Fabrication, and Transport Properties*"
J. Yu, S. Chung, and J.R. Heath, J. Phys Chem. B 2000, 104, 11864-11870

[20] "*Direct Growth of Amorphous Silicon Oxide Nanowires and Crystalline Silicon Nanowires from Silicon Wafer*"
S.Jin, Q. Li and C.S. Lee , Phys Stat Sol (a) 188, No. 2 R1-R2 (2001)

[21] "*Dependence of the silicon nanowire diameter on ambient pressure*"
H.Z. Zhang, D.P.Yu, Y. Ding, Z.G. Bai, Q.L.Hang and S.Q. Feng, Applied Physics Letters 73,23 (1998) pp 3396-3398

[22] "*Synthesis of Large Areas of Highly Oriented Very Long Silicon Nanowires*"
W. Shi, H. Peng, Y. Zheng, N. Wang, N. Shang, Z. Pan, C. Lee and S. Lee , Adv Mater,2000, 12, No. 18, September 15 pp 1343-1345

[23] "*Growth process conditions of vertically aligned carbon nanotubes using plasma enhanced chemical vapor deposition*"
M. Chhowalla, K. B. K. Teo, C. Ducati, N. L. Rupesinghe, G. A. J. Amaratunga, A. C. Ferrari, D. Roy, J. Robertson, and W. I. Milne, Journal of Applied Physics, Vol. 90, No. 10, pp. 5308-5317

[24] "*Crystallisation of Silicon ideas*"
J. Robertson, Nature, vol 418, 4/7/2002, pp 30-31

[25] "*Surface Controlled Plasma Deposition and Etching of Silicon Near the Chemical Equilibrium*"
M. Heintze, W. Westlake and P.V. Santos , Journal of Non-Crystalline Solids 164-166 (1993) 985-988

[26] "*Microcrystalline Silicon Thin Film Transistors made by Plasma Enhanced Chemical Vapour Deposition*"
M.W.D. Froggatt, University of Cambridge Doctoral Thesis, 1998

[27] R.S.Wagner and C.J. Doherty
J. Electrochem Soc, 115, 93 (1968)

[28] "Nanometer-sized silicon crystallites prepared by excimer laser ablation in constant pressure inert gas"
. Yoshida, S. Takeyama, Y. Yamada and K. Muto, Applied Physics Letters Vol 68, (1999) pp 1772-1774

[29] "*Vapour Pressure of the Metallic Elements*" - C.B. Alcock
from "*Handbook of Chemistry and Physics*" 76th edition, Edited by D.R.Lide, Published by CRC Press Inc, 1995-1996

[30] "*Synthetic Control of the Diameter and Length of Single Crystal Semiconductor Nanowires*"
M.S. Gudiksen, J. Wang, and C.M. Lieber , J. Phys Chem. B 2001,105, pp 4062-4064

[31] "*Silicon quantum wire array fabrication by electrochemical and chemical dissolution of wafers*"
L.Canham, Appl. Phys Lett 57 (10), 3 September 1990 pp 1046-1048

[32] "A model for growth directional features in silicon nanowires"
T.Y. Tan, S.T. Lee and U. Gosele, Appl. Phys. A, 74 (202) pp 423-432

[33] "*Instructions for the use of the DP80 Plasma Deposition System*"
A J Flewitt, Cambridge University, Department of Engineering, 6th April 2002.

[34] Personal Communication, Junfeng Geng, 24th May 2002.
Cambridge University Department of Chemistry

[35] Personal communication, Ken Teo, 2nd May 2002.
Cambridge University, Department of Engineering

[36] Personal Communication, Professor J. Robertson
Cambridge University, Department of Engineering

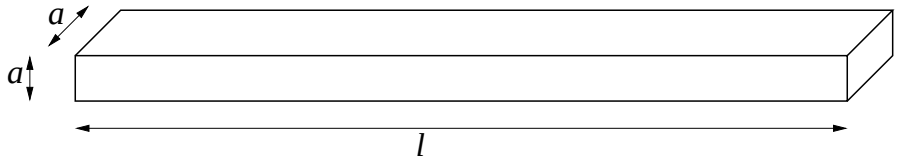
[37] Personal Communication, Dr. Andrew Flewitt 29th June and 30th August 2002.
Cambridge University, Department of Engineering

[38] Personal Communication, Stephan Hofmann
Cambridge University, Department of Engineering

A When is a Nanowire not a Nanowire?

The term "nanowire" is commonly used to refer to a long, thin structure, whose diameter is a few nanometers in size. However, the key property which makes them useful is quantum confinement, and that for quantum mechanical purposes, they are truly one-dimensional. What follows is an *approximate* calculation to illustrate the radius below which a wire becomes 1-dimensional.

Consider a nanowire approximated as a long, thin cuboid, of length l and of width and depth a, such that $l \gg a$. Assume that the electrons are free, i.e. that the Bloch contribution in the metal is ignored. (These approximations are crude, but they simplify the mathematics.)



The electrons have total energy E and potential energy V where $V = 0$ inside the box, and $V = \infty$ outside it. This is the standard "particle in a box" problem, and the Schrödinger equation may be solved for the energy levels. The Schrödinger equation is:

$$-\frac{\hbar^2}{2m}\nabla^2\Psi = (E - V)\Psi$$

This separates into 3 equations each in 1-d, and can be exactly solved to obtain:

$$\Psi = \sqrt{\frac{8}{a^2 l}} \sin\left(\frac{n_x \pi x}{l}\right) \sin\left(\frac{n_y \pi y}{a}\right) \sin\left(\frac{n_z \pi z}{a}\right)$$

and:

$$E = \frac{\pi^2 \hbar^2}{2m}\left[\left(\frac{n_x}{l}\right)^2 + \left(\frac{n_y}{a}\right)^2 + \left(\frac{n_z}{a}\right)^2\right]$$

where $k = \frac{n\pi}{l}$ and $n_i = [1, \infty]$

For the wire to be 1-D, we require that many modes are possible in the x-direction, but that only the $n = 1$ mode is possible along the y- and z-directions, the others being frozen out. This imposes a maximum value on E :

$$E < \frac{\hbar^2 \pi^2}{2m}\left[\left(\frac{1}{l}\right)^2 + \left(\frac{2}{a}\right)^2 + \left(\frac{1}{a}\right)^2\right]$$

and, since $l \gg a$:

$$E < \frac{5\hbar^2 \pi^2}{2m}\left(\frac{1}{a}\right)^2$$

The energy that an electron actually has is composed of two parts: thermal energy and ground state (zero-point) energy:

- Thermal energy $= \frac{3}{2}kT$

- Ground state energy: $E_{1,1,1} = \frac{\hbar^2\pi^2}{2m}\left(\frac{1}{l^2} + \frac{2}{a^2}\right)$

For a nanowire, the actual energy is less than the maximum energy:

$$\frac{3}{2}kT + \frac{\hbar^2\pi^2}{2m}\left(\frac{1}{l^2} + \frac{2}{a^2}\right) < \frac{5\hbar^2\pi^2}{2m}\left(\frac{1}{a}\right)^2$$

which gives:

$$a^2 < \frac{\hbar^2\pi^2}{kTm_e}$$

This is the approximate limit on the maximum diameter of a 1-d quantum nanowire. Note that a is inversely proportional to the square-root of the temperature. Thus the approximate limits on a quantum-confined nanowire are:

Temperature (K)	**Maximum radius of nanowire (nm)**
0	unlimited
1	98
298	6
1683 (Si melts)	2.2
31 000	1

These numbers are sensible to within an order of magnitude. However the model is over simplified: the electrons are neither free, nor of uniform energy. The higher energy electrons in the tail of the thermal energy spectrum (with perhaps $\frac{6}{2}kT$ rather than $\frac{3}{2}kT$ of energy) make the radii given above an overestimate. The lower effective mass of the non-free electrons has the opposite effect. Fortunately, in a nanowire only a few hundred atoms in diameter, neglection of defects is justified.

B Why do Nanoscale (Quantum-confined) Silicon Structures Emit Light?

Bulk silicon (which has an indirect bandgap) is an exceptionally poor and inefficient light-emitter. Light emission is much more efficient from porous silicon, silicon nanowires, or silicon nanocrystals, all of which have quantum-confinement on the scale of 1-3 nm. An explanation of why this is the case follows; as in appendix A, this is intended to be an *illustration*, not a full derivation.

Normal silicon is an indirect-bandgap semiconductor. The bandstructure shown in figure 51 illustrates how direct (photon-emission) transitions (A) are energetically unfavourable, compared to indirect (phonon-absorption + photon emission) transitions (B) which are energetically favoured. However, phonon absorption is a random process, therefore light emission is limited by the rate at which suitable phonons can arrive.

Consider a nanowire with diameter d and crystal lattice parameter a. In a normal (effectively infinite) crystal, $d \sim \infty$, so the only possible periodicity comes from the lattice: this is $\frac{\pi}{a}$ and is the Brillouin Zone. However, in a nanowire, there is an additional source of periodicity due to reflections at the

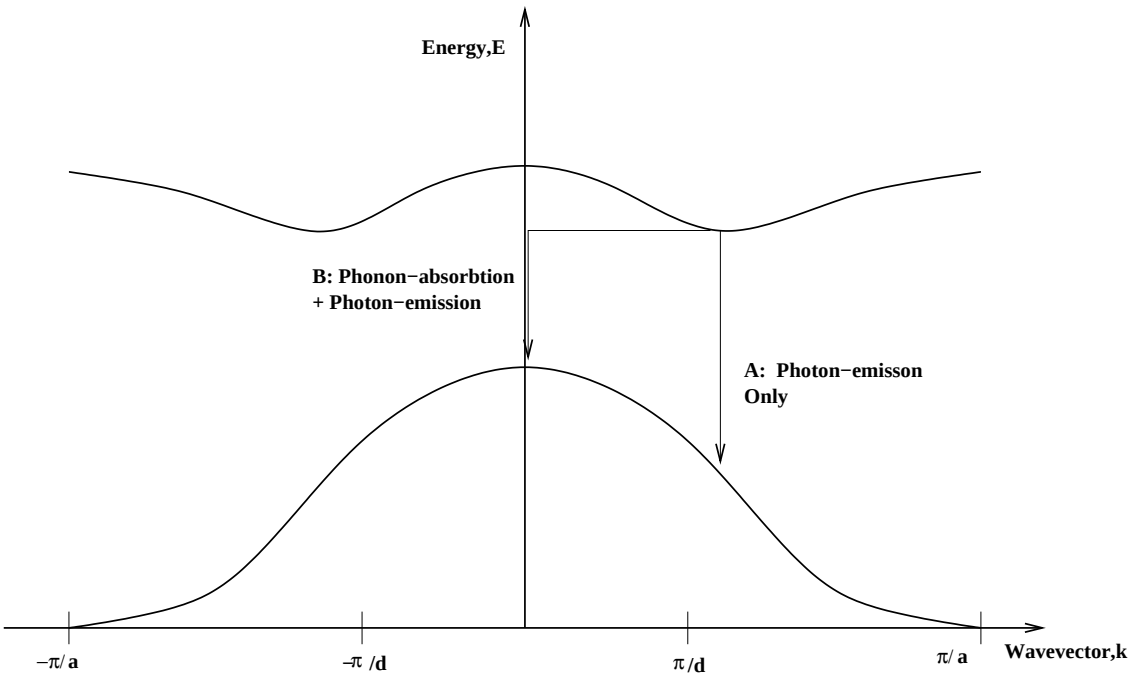


Figure 51: A schematic to show how indirect bandgap silicon has inefficient photon emission. The size of the crystal lattice is a.

boundaries. Therefore *in addition* to folding over at the zone boundary, the band structure must fold over at $\frac{\pi}{d}$. The new bandstructure is shown in figure 52.

In the case of a 1 nm nanowire, $a \simeq 0.1$nm and $d \simeq 1$nm, so the folding is in a region 1/10th the size of the 1st Brillouin zone. The lowest energy transition can now occur without the need for phonon absorbtion and the bandgap has become direct: the selection rules for optical emission are changed by the quantum-confinement and an indirect-gap semiconductor can now emit light. A side effect is that the bandgap is increased and so the emission from Si moves from the infrared (0.9 eV) to the visible (2-3 eV)[3]. However, an energy-wasting phonon process is still required: this makes the Si LEDs inefficient and, unless fabricated for stimulated (laser) emission, slow.

C How to Recognise a Good Silicon Nanowire Specimen

Of the various samples that come out of the DP80 deposition system, it is possible, with experience, to recognise which samples are likely to have nanowires and which do not. The following guide may be useful to anyone who continues the work of this thesis.

- Samples which are shiny, and usually silvery have a thick layer of amorphous-Si. If the surface appears cratered like the surface of the moon, this is due to de-lamination (the film is stressed), showing that the film is very thick. In either case, there are no nanowires, or if there are, they are buried.
- Samples which are dull, khaki/olive-coloured brown are likely to have nanowires. The surface is dull because light is scattered by the mesh of nanowires, since they are rough on the scale of

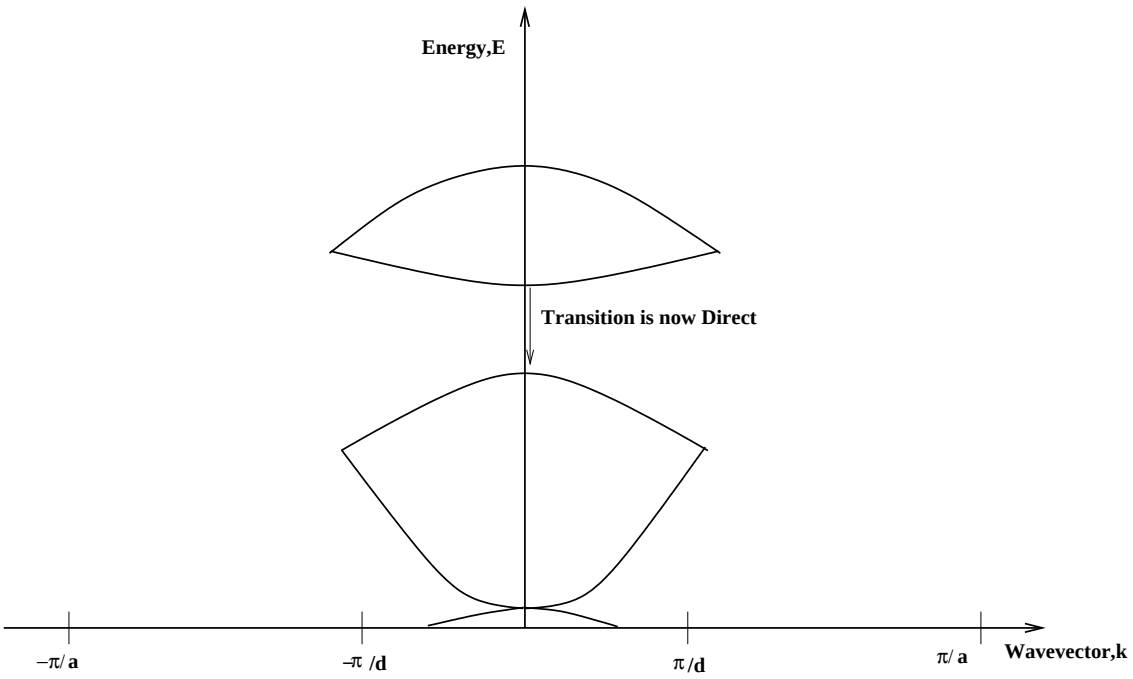


Figure 52: The bandstructure in the nanowire is folded over at π/d .

the wavelength of light. In general, the darker the colour, the better. In general, a dark, opaque colour implies tubes, wires, or a highly amorphous structure.

- The surface should be easily scratched - it should not wipe off with a light touch (in the way that the 1 nm Au does), but it should be quite easy to scratch with metal tweezers. If the surface is very hard, it often indicates a lot of amorphous silicon.

- If a quartz disc has been processed, it should be possible to see light through it: it should appear a dark reddish-brown in colour. (This is the colour of amorphous silicon.)

- Some of the better samples, with long wires can actually be seen in an optical microscope. The microscope in the clean-room, (with a 1 μm graticule) is easily able to see them, if they are long. (The surface of a nanowire is reflective, so it appears wider than it really is, and therefore is visible.) However shorter, or less densely packed nanowires are very hard to spot.

- In a Scanning Electron Microscope (SEM), the best place to see the wires is at the edge of the Au pattern, or where a crocodile clip masked the sample from Au in the evaporator. Alternatively, the sample may be scratched.

- There is an element of luck: successful "recipes" do fail randomly for about 1 sample in 10. Therefore a lack of nanowires doesn't *always* indicate the wrong conditions.